AROD TRANSPONDER

FINAL ENGINEERING REPORT

PREPARED FOR

THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GEORGE C. MARSHALL SPACE FLIGHT CENTER

UNDER CONTRACT NO. NAS8-5480

JUNE 1964

SPACE CRAFT, INC.

8620 S. MEMORIAL PARKWAY

HUNTSVILLE, ALABAMA

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I. INTRODUCTION

This Final Engineering Report is submitted in accordance with requirements of Contract No. NAS8-5480, under which the AROD Transponder was designed and developed by Space Craft, Inc. for the National Aeronautics and Space Administration.

The overall design requirements are discussed with particular emphasis on the unusual and difficult aspects of these requirements. Where new or unorthodox techniques were required or used, a detailed description of the methods and of the results obtained is included.

The Transponder circuits are described thoroughly from functional requirements to practical design and adjustment details. To facilitate organization and continuity, the detailed descriptions of the Transponder Receiver and Transponder Exciter circuits are arranged and listed in the text by modules corresponding to the block diagrams and to the actual hardware packaging. Block diagrams and schematics of all circuits are included at the end of Section V. The accompanying list of diagrams is arranged in numerical sequence according to the SCI drawing number.

Typical test data is included to illustrate the results

obtained and the performance to be expected from various functional parts of the Transponder.

Finally, a brief summary of the conclusions reached, performance obtained, problem areas, and recommendations is included.

SECTION II

EQUIPMENT PERFORMANCE REQUIREMENTS

AROD

Airborne Range and Orbit Determination

TRANSPONDER UNITS
GENERAL SPECIFICATIONS

NO. AROD-SPEC-10

DATE 27 August 1963

APPROVED Grady H. Saucier

ASTRIONICS DIVISION

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

1. SCOPE

1.1. Applicability. This specification sets forth the general requirements for system development models of AROD transponder equipment, and is applicable to all such equipment.

2. APPLICABLE DOCUMENTS

2.1. Documents. The following documents provide additional information as to requirements toward which design efforts should be directed since these requirements will be imposed on later models of the equipment:

(a) MSFC-STD-154	Printed Circuit Design and Construction; Standard for
(b) MSFC-PROC-158B	Soldering of Electrical Connections (High Reliability); Procedure for
(c) MSFC-PROC-257	Conformal Coating of Printed Circuit Assemblies; Procedure for
(d) AROD-SPEC-4	Transponder Equipment Tentative Environmental Test Specification

2.2. Availability. Copies of the above listed documents, for use in connection with AROD System contracts, may be obtained from the Contracting Officer.

3. REQUIREMENTS

3.1. Background. The system development models of AROD transponder equipment will be used for tests in the laboratories, and will also be operated at field sites during aircraft flight tests of the system. They will not be used in conjunction with vehicle launches or subjected to unusual site conditions. Thus it is not necessary that these units meet the requirements for flight-associated hardware. It is intended, however, that the prototype and production models to be later developed as a result of the system development test program, will meet all the requirements for flight-associated hardware to be operated under a variety of environmental conditions. All designs for system development units will be developed with this objective in mind.

3.2. Dimensions and Weight. Units shall be of such size that they can be mounted on standard 19 inch rack panels. Good design and manufacturing practices shall be followed, so that the units are not excessively large or heavy.

3.3. Packaging and Mounting. Units shall be mounted on standard 19 inch rack panels which are finished in dark grey metallic enamel. They shall have pull-out provisions for ease of testing and maintenance. Suitable pull-out handles shall be provided on each unit.

3.4. Environmental Requirements. Units shall meet conditions which would normally be encountered in laboratory and field site testing conditions.

3.4.1. Temperature. The equipment shall be capable of normal operation in atmosphere at 0° to + 60° C.

3.4.2. Shock and Vibration. The equipment shall be designed to withstand the normal shocks which would be encountered in shipping and handling, laboratory testing, and field site testing.

3.5. Power Requirements. The equipment shall be designed to operate from 120 ± 12 volts, 60 Hz AC power.

3.6. Connectors.

3.6.1. Signal Connectors. Unless otherwise specified in individual instances, all signal connectors shall be type TNC or type N.

3.6.2. Power and Distribution Connectors. All power and distribution connectors shall be AN or MS approved types.

3.7. Test Points. Test points shall be provided as required by specifications for individual units. Additional test points may be added as considered advisable. Test points associated with signal paths shall be green; all others shall be white.

3.8. Monitoring Points. Monitoring points shall be provided as required by specifications for individual units. Additional monitoring points which are considered to be required to provide complete information of important system characteristics shall be added.

3.8.1. Monitoring Outputs. A DC output proportional to the function being measured, and of such magnitude as to be suitable for recording by oscillograph, shall be provided for each monitoring point.

3.8.2. Monitoring Connections. All monitoring points shall be connected to a common connector for each unit.

3.9. Components. All components used shall conform to accepted standards of the industry.

3.10. Design. All units shall meet accepted standards of performance and reliability.

3.11. Manufacturing. All units shall conform to accepted standards of workmanship. Components shall not be potted.

3.12. Design Objectives. All design shall be accomplished with the following requirements in view. While these requirements are not binding upon the equipment covered under this specification, no design shall be used which will not allow compliance with these requirements in future models.

3.12.1. Dimensions and Weight. Future units will be required to be of the minimum size and weight which is consistent with meeting the requirements for reliable equipment.

3.12.2. Environmental Requirements. Future units will be required to meet

the environmental test requirements for launch-and-space vehicle associated equipment; the tentative environmental testing these units will be required to meet is contained in AROD-SPEC-4.

3.12.3 Components. Future units will be required to incorporate only components which meet the reliability and quality requirements for use in manned vehicle systems.

3.12.4. Manufacturing. Future equipment will be required to comply with MSFC-STD-154, MSFC-PROC-158B, and MSFC-PROC-257.

AROD

Airborne Range and Orbit Determination

TRANSPONDER TRACKING EQUIPMENT

NO. AROD-SPEC-11

DATE 22 October 1963

APPROVED Bradley H. Saunders

ASTRIONICS DIVISION

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

1. SCOPE

1.1. This specification is applicable to the system development model of the Transponder Tracking Equipment.

2. APPLICABLE DOCUMENTS

2.1. The following document sets forth requirements applicable to the ground-based AROD equipment:

AROD-SPEC-11 Transponder Units, General Specifications

3. REQUIREMENTS

3.1. General.

3.1.1. Background. The Transponder Tracking Equipment shall perform the following functions:

(a) Receive the phase modulated signal transmitted by the vehicle-borne equipment.
(b) Amplify and demodulate the ranging tones on the received signal with minimum degradation to the input signal-to-noise ratio.
(c) Prepare the demodulated signal for retransmission by removing as much noise as possible by use of narrow band filters and phase-lock loops.
(d) Synthesize for retransmission a carrier signal that is shifted in frequency but coherent with the received carrier frequency.
(e) Modulate the extracted range tones onto the coherent carrier signal.
(f) Provide means for modulating one of the range tones with information which is to be sent to the vehicle-borne equipment.
(g) Provide the capability for the selection of one of four carrier frequencies.
(h) Provide for quick acquisition of the received frequency as a result of information obtained from the command link.
(i) Provide for quick acquisition by the vehicle-borne equipment by providing for doppler compensation in the generation of the transponder tracking carrier frequency.
(j) Provide for control of the operation of this equipment by means of inputs from the command link.

3.1.2. Description. The Transponder Tracking Equipment shall consist of the gound-based tracking receiver, frequency synthesizer, and tracking transmitter of the AROD System. The rf amplifier and the 1st mixer of the receiver and the output stage of the transmitter are not included as a part of this specification.

3.2. Performance characteristics. The equipment shall meet the following performance requirements:

(a)	Phase characteristics	
	Linearity	±2.0% within operational bandwidth
	Stability	±1.0° of differential phase shift between carrier and each range tone over temperature limits of 0° to 60°C.
(b)	Noise figure	7.0 db

(c)	Dynamic range	50 db
(d)	Carrier phase-lock loop	
	Effective noise bandwidth	300 Hz
	Dynamic tracking rate	3.5 kHz/sec
	Stability of VCO	
	Short term	1 part in 10^8/1.0 msec
	Long term	3 parts in 10^9/day or 1 part in 10^6/day
(e)	Acquisition time of transmitter tracking filter	
	Loop containing reference oscillator and VCO #2	0.5 sec
	Loop containing VCO #1 and VCO #2	0.5 sec

3.3 Input from first mixer. The first IF amplifier shall accept the following received signal input from the first mixer:

(a)	Center frequency	103.048 MHz
(b)	Frequency variation-maximum	±80 kHz
(c)	Power-minimum	-120.0 dbm
	maximum	-70.0 dbm
(d)	Bandwidth-3.0 db	5.6 MHz
	80.0 db	±57.5 MHz
(e)	Input impedance	50 ohms
(f)	Connector	Type TNC
(g)	Number of connectors	1

3.4. Input from command receiver. This equipment shall accept the following inputs from the command receiver:

(a)	Center frequency	28.104 MHz
(b)	Frequency variation- maximum	±1.0 kHz
(c)	Power	0 dbm, ±1.0 db
(d)	Impedance	50 ohms
(e)	Connector	Type TNC
(f)	Number of connectors	1

The above input shall be used to set the frequency of the tracking receiver for the purpose of acquiring the tracking signal transmitted from the vehicle.

3.5. Input from command logic. This equipment shall accept the following inputs from the command logic.

3.5.1. STANDBY Input Signal. This equipment shall accept a signal from the command logic equipment, designated as STANDBY, which will control the application of equipment operating power. Operating power shall be applied to this equipment at all times except during the OFF mode. The signal is described as follows:

(a)	Frequency	DC
(b)	Amplitude	
	Operating power ON	5.5±0.5 v
	Operating power OFF	0.25±0.25 v
(c)	Input impedance-minimum	500 ohms
(d)	Connectors	Type TNC
(e)	Number of Connectors	1

3.5.2. FREQUENCY SELECTION input signals. This equipment shall accept signals from the command logic, designated as FREQUENCY SELECTION, which will determine which one of the four carrier frequencies is used. These signals are described as follows:

(a)	Frequency	DC
(b)	Amplitude	
	Carrier ON	5.5±0.5 v
	Carrier OFF	0.25±0.25 v
(c)	Input impedance-minimum	500 ohms
(d)	Carrier designation	
	Channel one	2211.7848 MHz
	Channel two	2213.1900 MHz
	Channel three	2218.5766 MHz
	Channel four	2219.9818 MHz
(e)	Connector	Type TNC
(f)	Number of connectors	4

3.5.3. RANGE TONE GATE input signal. This equipment shall accept a signal from the command logic, designated as RANGE TONE GATE, which will control when the two lower ranging tone signals are OFF or ON. This signal also determines the source of the medium fine ranging tone. It is described as follows:

(a)	Frequency	DC
(b)	Amplitude	
	Lower ranging tones ON; Coherent medium fine ranging tone selected	5.5±0.5 v
	Lower ranging tones OFF; Non-coherent medium fine ranging tone selected	0.25±0.25 v
(c)	Input impedance-minimum	500 ohms
(d)	Connector	Type TNC
(e)	Number of connectors	1

NOTE: The amplitude of the non-coherent medium fine range tone shall be independently adjustable.

3.5.4. SITE IDENTIFICATION MODULATION input signal. This equipment shall accept a signal from the command logic, designated as SITE IDENTIFICATION MODULATION, which will contain certain information to be modulated onto the medium fine ranging tone. This signal is described as follows:

(a)	Pulse repetition rate	1.0 kHz (NRZ)
(b)	Pulse width	1.0 millisecond
(c)	Amplitude	
	Logical "1"	5.5±0.5 v
	Logical "0"	0.25±0.25 v
(d)	Degradation to rise and fall time of input pulse-maximum	10 microseconds
(e)	Input impedance-minimum	500 ohms
(f)	Connector	Type TNC
(g)	Number of connectors	1

3.5.5. DOPPLER COMPENSATION GATE input signal. This equipment shall accept a signal from the command logic, designated as DOPPLER COMPENSATION GATE, which will control when the Doppler compensation is placed on the retransmitted carrier signal. The input signal is described as follows:

(a)	Frequency	DC
(b)	Amplitude	
	Doppler compensation ON	5.5±0.5 v
	Doppler compensation OFF	0.25±0.25 v
(c)	Input impedance-minimum	500 ohms
(d)	Connector	Type TNC
(e)	Number of connectors	1

3.6. Output to 1st mixer. This equipment shall provide an output signal which will be used as the local oscillator for the 1st mixer. The signal is described as follows:

(a)	Frequency	2173.376 MHz
(b)	Frequency variation-maximum	±80 kHz
(c)	Power	0 dbm ±1.0 db
(d)	Output impedance	50 ohms
(e)	Connector	Type N
(f)	Number of connectors	1

3.7. Output to tracking transmitter. This equipment shall provide an output to the tracking transmitter. This output will be at one of the four carrier frequencies and will also contain the lower sidebands of the modulating tones. The output signals are described as follows:

Carrier (f_{ci}): i = 1, 2, 3, and 4

Frequency	
Channel 1	2211.7848 MHz
Channel 2	2213.1900 MHz
Channel 3	2218.5766 MHz
Channel 4	2219.9818 MHz
Power-maximum	2.86 millwatts, ±1.0 db
Range of variation	+1.0 db, -10.0 db

Sideband derived from the $F_{r1} - F_{r2}$ modulating tone

Frequency	$f_{ci} - (F_{ri} - F_{r2})$
Power-maximum	1.43 millwatts, ±1.0 db
Range of variation*	+1.0 db, -10.0 db

Sideband derived from the F_{r1} modulating tone

Frequency	$f_{ci} - F_{r1}$
Power-maximum	2.86 milliwatts, ±1.0 db
Range of variation*	+1.0 db, -10.0 db

Sidebands derived from the $F_{r1} \pm f_1$ modulating tone

Frequency	$f_{ci} - (F_{r1} \pm f_1)$
Power-maximum	0.71 milliwatts, ±1.0 db
Range of variation*	+1.0 db, -10.0 db

Sidebands derived from the $F_{r1} \pm f_2$ modulating tone

Frequency	$f_{ci} - (F_{r1} \pm f_2)$
Power	0.71 milliwatts, ±1.0 db
Range of variation*	1.0 db, -10.0 db

*The range of amplitude variation and the phase delay of F_{r1}, $F_{r1} - F_{r2}$, and the combination of f_1 and f_2 shall be independently adjustable.

Output impedance	50 ohms
Connectors	Type TNC
Number of connectors	1

NOTE: The frequencies represented by the various symbols are listed as follows:

F_{r1} = 2.342 MHz
F_{r2} = 73.1875 kHz
F_{r3} = 2.287 kHz
F_{r4} = 71.47 Hz

f_1 = 1.10782 kHz

f_2 = 1.17929 kHz

3.8. Monitoring points. Monitoring points shall be provided as required by AROD-SPEC-10 for recording by an oscillograph or monitoring by a function meter. The signals to be monitored in this manner are listed as follows:

(a) First mixer current
(b) AGC of 1st IF
(c) Acquisition by VCXO #1
(d) Acquisition by VCXO #2
(e) Range tones f_1 and f_2
(f) Range tone F_{r1}
(g) VCXO # 1 control voltage
(h) VCXO #2 control voltage
(i) Noise detector output
(j) Range tone ON-OFF switch (1A)
(k) Doppler translation switch (2A)
(l) Modulated range tone $F_{r1} - F_{r2}$
(m) VCXO #3 control voltage
(n) FREQUENCY SELECTION input signal-channel 1
(o) FREQUENCY SELECTION input signal-channel 2
(p) FREQUENCY SELECTION input signal-channel 3
(q) FREQUENCY SELECTION input signal-channel 4

In addition the AC input voltage and all input DC voltages shall be connected to the monitoring point connector; no signal processing is required on these voltages.

3.9. Test points. Test points shall be provided and color coded as required by AROD-SPEC-5. Unless the performance of the equipment will be adversely affected, test points shall be provided for the following:

3.10.1. IF AMPLIFIER

(a) AGC of 1st IF amplifier
(b) Output 103.048 MHz IF amplifier
(c) Local oscillator for 2nd mixer
(d) Output 14.052 MHz IF amplifier

3.10.2. DEMODULATOR

(a) Input from sideband IF amplifer
(b) Input from carrier IF amplifier
(c) Control voltage for VCO #1
(d) Input from command receiver VCO
(e) Acquisition sensor

3.10.3. RANGE TONE CIRCUITS

(a) Input from product detector
(b) Control voltage of VCO #3
(c) Control voltage of VCO #3B
(d) 2.342 MHz range tone (between variable phase shifter and mixer)
(e) Input to range tone ON-OFF switch (1A)
(f) Each of the three inputs to linear adder

3.10.4. TRANSMITTER TRACKING FILTER

(a) Control voltage for VCO #2
(b) Input to doppler translation switch (2A)
(c) Input from command receiver VCO
(d) Output reference oscillator

3.10.5. TRANSMITTER SYNTHESIZER

(a) Output of 1.171 MHz VCO
(b) Control voltage of 1.171 MHz VCO
(c) Input from VCO #2
(d) Output of 22.249 MHz PCO
(e) Output of MHz PCO
(f) Output of spectrum generator
(g) Output of lower sideband filter
(h) Two inputs to output mixer
(i) Output of output mixer
(j) Four channel selection gates
(k) Control voltage of 22.249 MHz VCO
(l) Control voltage of 70.26 MHz VCO
(m) Control voltage of 5.6208 MHz to 13.817 MHz VCO

Additional test points shall be provided as deemed advisable for checking the performance of the equipment.

SECTION III

AROD TRANSPONDER

THEORY OF OPERATION

(UNDER SEPARATE COVER)

SECTION IV

SYSTEM DESIGN CONSIDERATIONS

IV. SYSTEM DESIGN CONSIDERATIONS

4.1 Threshold Signal and Noise Calculations

The receiver noise figure will be:

$$F_{RX} = F_F + \frac{F_A + 1}{G_F} + \frac{F_m - 1}{G_F G_A} + \frac{F_{IF} - 1}{G_F G_A G_M} =$$

$$1 + .83 + .10 + .27 = 2.2 \text{ (or } 3.4 \text{ db)}$$

for the following system parameters:

F_F = 1 (0 db) preselector filter noise figure

F_A = 1.66 (2.2 db) Para. Amp. noise figure

F_M = 5 (7 db) Mixer Noise Figure

F_{IF} = 3.16 (5 db) First I.F Amp. Noise Figure

G_F = 0.795 (-1 db) Preselector Filter Gain

G_A = 50 (17 db) Para. Amp. Gain

G_M = 0.2 (-7 db) Mixer Gain

Therefore, the receiver noise temperature will be:

$$T_{eq} = T_o (F - 1)$$

$$T_{RX} = 290 (2.2 - 1) = 350^{\circ}K$$

Assuming 0 db antennas at 2276 megacycles, one half of the antenna

solid angle will see a 290°K earth and the other half will see about a 29°K sky. Thus the antenna temperature will be:

$$T_{ANT} = (290 + 29)/2 = 160^{\circ}K$$

The receiving system temperature will then be:

$$T_{SYS} = T_{RX} + T_{ANT} = 350 + 160 = 510^{\circ}K$$

and the equivalent input noise power will be:

$$N = -171.5 \text{ dbm/cycle } (510^{\circ}K)$$

The minimum carrier power input can be calculated knowing the maximum range (1000 N. miles), carrier power radiated (3.076 watts), antenna gains (0 db), and frequency:

$$P_r = \frac{P_T G_T G_R{}^2}{(4\pi R)^2}$$

assuming $G_T = G_R = 1$

$$P_{r_{min}} = \frac{(3.076)(1)(1)\left(\frac{300}{2276}\right)^2}{(4 \times 3.14 \times 1.852 \times 10^6)^2}$$

$$= .985 \times 10^{-16} \text{ watts}$$

$$= -130.06 \text{ dbm}$$

Therefore, minimum carrier to noise ratio at the receiver input is:

$$\frac{C}{N} = \frac{-130.06 \text{ dbm}}{-171.5 \text{ dbm/cycle}} = 41.4 \text{ db/cycle}$$

The carrier main loop noise bandwidth is 300 cycles. This is a 24.8 db increase above a one cycle noise bandwidth. Therefore, the minimum carrier to noise ratio in the carrier loop will be:

$$\frac{C}{N} = +16.6 \text{ db}$$

The noise bandwidth from the receiver input to the input of the carrier crystal filter is approximately 10 megacycles. This is a 70 db increase above a 1 cycle bandwidth. Assuming that the bandwidth to this point is determined solely by the IF amplifiers, the minimum carrier to noise ratio at the crystal filter input is:

$$\frac{C}{N} = -28.6 \text{ db}$$

The approximate noise bandwidth to the carrier crystal filter is 17 kilocycles. This is a 42.3 db increase above a 1 cycle bandwidth. The minimum carrier to noise ratio at the filter output, then, is:

$$\frac{C}{N} = -0.9 \text{ db}$$

Since only linear and relatively wideband amplifiers are employed between the carrier crystal filter and the coherent amplitude detector in the AGC Demodulator, the minimum carrier to noise ratio at the detector input is -0.9 db. However, the limiter in front of the main loop phase detector, with this $\frac{C}{N}$ input, will cause an improvement in the carrier to noise ratio of 0.6 db (see Journal of Applied Physics, June 1963, Page 725). Therefore, the minimum carrier to noise ratio at the input to the main loop phase detector is:

$$\frac{C}{N} = -0.3 \text{ db}$$

The noise bandwidth from the receiver input to the input of the sideband crystal filters is approximately 14 megacycles (again assuming that the bandwidth is determined solely by the IF Amplifiers). If the total sideband power transmitted by the Vehicle Transmitter is 6.921 watts, the total signal (including the carrier) to noise ratio at the input to the sideband filters is approximately:

$$\frac{S_T}{N} = \frac{+46.5 \text{ db}}{\text{cycle}}$$

and, in the 14 megacycle bandwidth:

$$\frac{S_T}{N} = -25.0 \text{ db}$$

The carrier, however, does not appear at the output of the sideband filters. The combined noise bandwidth at the output of the filters is approximately 61 kilocycles. The minimum total sideband to noise ratio at the filter output, and consequently at the input to the Range Tone Circuit, is:

$$\frac{SB}{N} = -2.92 \text{ db}$$

The 2.342 megacycle range tone loop is locked on the 2.342 megacycle sideband which is approximately 3.5 db below the total sideband power. Therefore, the minimum signal to noise ratio at the input to the 2.342 megacycle phase detector, for all practical purposes, is:

$$\frac{F_{R1}}{N} = -6.4 \text{ db}$$

The phase detector in the 2.268 Range Tone Circuit is preceeded by a limiter. The total $\frac{SB}{N}$ ratio at the limiter input is -2.92 db. The limiter, with this particular input, will degrade the signal to noise ratio by approximately .45 db. Therefore, the minimum total $\frac{SB}{N}$ ratio at the input to the phase detector is -3.37 db. The 2.268 megacycle sideband is approximately 9.53 db below the total sideband power. Therefore, the minimum signal to noise ratio at the input to the 2.268 megacycle phase detector, for

all practical purposes, is

$$\frac{f_3}{N} = -12.9 \text{ db}$$

The noise bandwidths of both the 2.342 and the 2.268 megacycle phase locked loops is approximately 100 cycles. The signal to noise improvement due to the noise bandwidth reduction is equal to the inverse of the bandwidth ratios. Therefore, the signal to noise through the two loops will be improved by

$$\frac{6.1 \times 10^4}{10^2} = 6.1 \times 10^2, \text{ or } 27.86 \text{ db.}$$

The minimum signal to noise ratio, then, at the output of the 2.342 megacycle phase locked loop is:

$$\left(\frac{F_{R1}}{N}\right)_{out} = +21.5 \text{ db}$$

and the minimum signal to noise ratio at the output of the 2.268 megacycle phase locked loop is:

$$\left(\frac{f_3}{N}\right)_{out} = +14.96 \text{ db.}$$

4.2 Phase Locked Loop Calculations

The following paragraphs are devoted to the calculations used in the AROD Transponder phase locked loops. Empha-

sis is placed upon the main receiver loop because of its importance within the system.

4.2.1 Main Receiver Loop

A simplified block diagram of the main receiver loop is shown in Figure 9 in the Theory of Operation. The loop has the closed loop transfer function:

$$H(S) = \frac{1 + \tau_2 S}{1 + (\frac{1}{GA} + \tau_2)S + \frac{\tau_1}{G} S^2} \qquad (4.1)$$

and may be simplified to:

$$H(S) = \frac{1 + \tau_2 S}{1 + \tau_2 S + \frac{\tau_1}{G} S^2} \qquad (4.2)$$

where:

τ_1 and τ_2 are the loop filter time constants.

A = Loop filter DC gain.

G = Open loop gain = $360\ K_D K_V K_M\ \text{sec}^{-1}$.

K_D = Phase detector gain in volts/degree.

K_V = VCO gain in cps/volts.

K_M = Multiplier gain.

The main receiver loop shown in Figure 9 actually consists of three loops within each other. The derivation of equation 4. 1 from these three loops may be performed by referring to an equivalent block diagram shown in Figure 4-1. The inside loop composed of the phase detector, filter, VCO, and multiplier K_{M3} has the transfer function:

$$H''(S) = \frac{H_o''(S)}{1 + H_o''(S)} = \frac{C''(S)}{R''(S)} \qquad (4.3)$$

where the open loop transfer function is $H_o''(S)$ and $R''(S)$ and $C''(S)$ are the Laplace transformed input and output functions, respectively, and

$$H_o''(S) = 360 \ \frac{1}{S} \ K_V K_D K_{M3} \ F(S)$$

or

$$H_o''(S) = K \ K_{M3} \ \frac{1}{S} \ F(S)$$

where

$$K = 360 \ K_V K_D$$

$F(S)$ = Loop filter transfer function.

Substituting the equations above in equation 4. 3 yields

$$H''(S) = \frac{K \ K_{M3} \ F(S)}{S + K \ K_{M3} \ F(S)} \qquad (4.4)$$

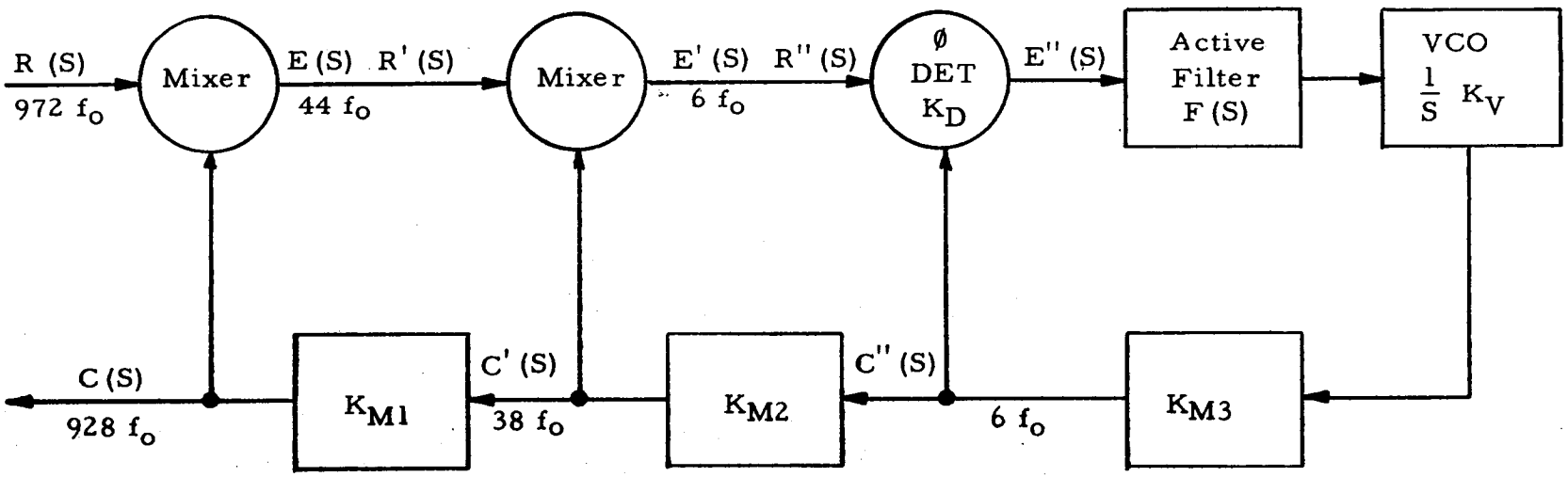

FIGURE 4-1. MAIN RECEIVER LOOP EQUIVALENT BLOCK DIAGRAM

The inside loop may now be replaced by one block with the transfer function given in equation 4.4. The same process may be used to simplify the analysis further.

$$H_o'(S) = K_{M2}\ H''(S)$$

$$H'(S) = \frac{C'(S)}{R'(S)} = \frac{H_o'(S)}{1 + H_o'(S)} = \frac{K_{M2}\, H''(S)}{1 + K_{M2}\, H''(S)} \qquad (4.5)$$

again

$$H_o(S) = K_{M1}\ H'(S)$$

$$H(S) = \frac{H_o(S)}{1 + H_o(S)} = \frac{K_{M1}\, H'(S)}{1 + K_{M1}\, H(S)} \qquad (4.6)$$

Combining equations (4.4), (4.5), and (4.6) yields:

$$H(S) = \frac{K\ K_{M1}\ K_{M2}\ K_{M3}\ F(S)}{S + K\ K_{M3} F(S)\ 1 + K_{M2} + K_{M1}\ K_{M2}} \qquad (4.7)$$

The values for K_{M1}, K_{M2} and K_{M3} are $24\frac{19}{80}$, $6\frac{1}{3}$ and $\frac{1}{2}$, respectively. Although equation (4.7) is in an exact form, it is somewhat cumbersome. Since $K_{M1}\ K_{M2}$ is much greater than $1 + K_{M2}$ the approximation shown in equation (4.8) may be made with negligible error.

$$H(S) = \frac{K\ K_{M1}\ K_{M2}\ K_{M3}\ F(S)}{S + K\ K_{M1}\ K_{M2}\ K_{M3}\ F(S)}$$

or

$$H(S) = \frac{K\ K_M\ F(S)}{S + K\ K_M F(S)} = \frac{GF(S)}{S + GF(S)} \qquad (4.8)$$

$$K_M = K_{M1}\ K_{M2}\ K_{M3} = 77\ 1/3$$

The active loop filter transfer function $F(S)$, can be shown to be

$$F(S) = \left| A\ \frac{1 + \tau_2 S}{1 + A\ \tau_1 S} \right| \qquad (4.9)$$

Substituting equation 4.8 in 4.9 yields equation 4.1. The simplification to equation 4.2 is made because τ_2 is much greater than $1/AG$.

Integrating the complex conjugate of equation 4.2 yields the loop noise bandwidth ($2B_L$) in terms of τ_1, τ_2 and G (this derivation is not included here because of its length). The subsequent selection of an optimum damping ratio of 0.707 results in the familiar equations stated below:

$$\tau_1 = \frac{9G}{32\ B_L^2} \qquad (4.10)$$

$$\tau_2 = \frac{3}{4\ B_L} \qquad (4.11)$$

τ_1 is the loop filter time constant consisting of the

product of the filter input resistance and the feedback capacitance. τ_2 is the product of the series feedback resistance and capacitance. The amplifier gain does not appear in these equations because it is cancelled out of the last term of the denominator of equation (4. 1).

The steady state phase error equations for step and ramp function inputs may be found using equation 4. 1. The error function E(S) in Figure 4. 1 is of primary interest in the loop analysis. Measurements at the first mixer output are not practical, however, whereas the phase errors at the detector output are easily measured. The three error functions in Figure 4-1, $E''(S)$, $E'(S)$, $E(S)$ are shown below to be practically identical, indicating that phase detector measurements are in fact, an accurate measurement of the loop error $E(S)$. From Figure 4-1

$$E(S) = R(S) - C(S) = R'(S)$$

$$E'(S) = R'(S) - C'(S) = R''(S)$$

$$E''(S) = R''(S) - C''(S)$$

and

$$C(S) = K_{M1}\, C'(S)$$

$$C'(S) = K_{M2}\, C''(S)$$

Combining the above equations and solving for $E''(S)$ yields

$$E''(S) = R(S) - C(S)\left[1 + \frac{1}{K_{M1}} + \frac{1}{K_{M1}\,K_{M2}}\right]$$

or

$$E''(S) \approx R(S) - C(S) = E(S) \qquad (4.12)$$

The error introduced from the above approximation is

$$1 + \frac{1}{K_{M1}} + \frac{1}{K_{M1}\,K_{M2}} = 1 + \frac{38}{928} + \frac{38}{928} \times \frac{6}{38} = 1.047$$

or less then 5%.

Equation 4.12 may be rewritten to enable steady-state error calculations from loop parameters.

$$E(S) = R(S) - C(S)$$

or
$$\frac{E(S)}{R(S)} = 1 - \frac{C(S)}{R(S)} = 1 - H(S) \qquad (4.13)$$

Substituting equation 4.1 in 4.13 and simplifying yields

$$\frac{E(S)}{R(S)} = \frac{\frac{1}{GA} + \frac{\tau_1}{G}\,S \quad S}{1 + \frac{1}{GA} + \tau_2 \quad S + \frac{\tau_1}{G}\,S^2} \qquad (4.14)$$

The steady-state phase error for a step frequency input can now be found by applying the final value theorem to equation 4.14,

$$\phi(t)_{SS} = \lim_{S \to 0} \; S \frac{E(S)}{R(S)} \frac{\Delta f}{S^2}$$

$$= 360 \frac{\Delta f}{GA} \quad \text{degrees} \qquad (4.15)$$

The steady-state error for a ramp frequency input can also be found,

$$\phi(t)_{SS} = \lim_{S \to 0} \; S \frac{E(S)}{R(S)} \frac{\dot{f}}{S^3}$$

$$= 360 \left[\frac{\tau_1 \dot{f}}{G} + \frac{\dot{f}}{AG} \lim_{S \to 0} \frac{1}{S} \right] \quad \text{degrees} \qquad (4.16)$$

The first term above is of interest in defining the steady-state errors. The magnitude of the second term increases with time and is insignificant under actual conditions.

Equations 4.15 and 4.16 were used to calculate the main loop errors tabulated in Table 4-1. The discussion immediately preceding illustrates the technique for obtaining experimental results for comparison with analytical data. Equations 4.10 and 4.11 were used to determine the filter time constants (see Table 4-1) for a loop noise bandwidth of 300 cps.

All of the preceding equations indicate that the loop gain, G, is a constant. This, however, is not the case. The use of a

LOOP DESIGNATION	INPUT FREQ MC	OUTPUT FREQ MC	VCO FREQ MC	OPEN LOOP MULT	$2B_L$ LOOP NOISE BW CPS	Δf MAX DOPPLER LOOP INPUT/CPS	$\dot{f}$ MAX DOPPLER RATE LP INP CPS/S	K_V VCO GAIN CPS/V	K_D DET GAIN V/RAD	K_M MULT GAIN	G OPEN LOOP GAIN SEC^{-1}	TYPE DC AMPL.	A DC AMPL GAIN	t MAX LOCK-IN TIME MS	$\phi_{ss}\ \Delta f$ MAX DOPPLER ERROR DEG.	$\phi_{ss}\ \dot{f}$ MAX ACCEL. ERROR DEG	FILTER TIME CONSTANTS T_1 MS	FILTER TIME CONSTANTS T_2 MS
Main Receiver Loop	(972fo) 2276.4	(928fo) 2173.3	(12fo) 28.104	None	300	.82K	3000	300	.00833	81	48,400	Active Filter	50	N/A	±12.2	13.5	605	5
RCVR Acquisition Loop	(12fo) 28.104	(12fo) 28.104	(12fo) 28.104	1/2	500	505	18.5	300	.0833	1/2	4,500	Active Filter	50	.0655	±.81	.03	20.2	3.0
XMTR Tracking Loop	(12fo) 28.104	(12fo) 28.104	(12fo) 28.104	None	1200	2020	37	300	.0933	1	9,000	None	N/A	.0755	± 40.5	.011	7.04	1.25
Med. Fine Range Tone Loop	2.268	2.268	2.268	None	100	84	3.085	120	.025	1	210	Active Filter	100	.23	±.44	.125	23.6	15
Fine Range Tone Loop	(fo) 2.342	(fo) 2.342	(fo) 2.342	None	100	84	3.085	120	.0167	1	720	Active Filter	100	.23	±.42	.125	81	15
RCVR Divide by 24 Loop	(12fo) 28.104	(1/2 fo) 1.171	(1/2 fo) 1.171	None	2000	1010	37	20	.0833	24	14,400	None	N/A	.0041	±25.2	.0038	4.05	0.75
XMTR Divide by 24 Loop	(12fo) 28.104	(1/2 fo) 1.171	(1/2 fo) 1.171	None	2000	2020	37	20	.0833	24	14,400	None	N/A	.016	±25.2	.0038	4.05	0.75
RCVR Synthesizer x58 Multiplier	(1/2 fo) 1.171	(29fo) 67.918	(14.5 fo) 33.959	58	1200	220	44.7	600	.125	1	27,000	None	N/A	.028	± 16.3	.0126	21	1.25
RCVR Synthesizer x76 Multiplier	(1/2 fo) 1.171	(38 fo) 88,996	(38 fo) 88.996	152	4000	6384	234.4	1000	.0333	2	24,000	DC amp	4	.0204	±24.0	.0423	6.75	0.375
XMTR Synthesizer x 57 Multiplier	(1/2 fo) 1.171	(28.5 fo) 66.747	(9.5 fo) 22.249	57	1500	1596	29.4	2000	.0833	1	60,000	None	N/A	.0242	± 4.8	.003	.30	1.0
XMTR Synthesizer x 60 Multiplier	(1/2 fo) 1.171	(30fo) 70.260	(30fo) 70.260	120	4000	10,080	183.2	1000	.0333	2	24,000	DC amp	4	.0506	± 18.9	.0046	6.75	0.375
Spectrum Gen. #1 x 4.8 Multiplier	(1/2 fo) 1.171	(2.4fo) 5.6208	(2.4fo) 5.6208	24	2000	2020	37	400	.0833	5	60,000	None	N/A	.0163	±6.06	.0037	16.9	0.75
Spectrum Gen #1 x 6.0 Multiplier	(1/2 fo) 1.171	(3.0fo) 7.0260	(3.0fo) 7.0260	30	2000	2520	46.2	600	.0833	5	90,000	None	N/A	.0254	±5.04	.0047	25.3	0.75
Spectrum Gen. #2 x 10.6 Multiplier	(1/2 fo) 1.171	(5.3fo) 12.4126	(5.3fo) 12.4126	53	3000	4450	82	1000	.0416	5	75,000	None	N/A	.0234	±10.7	.0037	9.4	0.50
Spectrum Gen. #2 x 11.8 Multiplier	(1/2 fo) 1.171	(1/2 fo) 13.8178	(5.9fo) 13.8178	59	3000	4960	91	1500	.0416	5	112,500	None	N/A	.0292	±7.94	.0041	14.1	0.50

TABLE 4-1 AROD TRANSPONDER LOOP CHARACTERISTICS

LOOP DESIGNATION	INPUT FREQ MC	OUTPUT FREQ MC	VCO FREQ MC	OPEN LOOP MULT	$2B_L$ LOOP NOISE BW CPS	Δf MAX DOPPLER LOOP INPUT/CPS	$\dot{f}$ MAX DOPPLER RATE LP INP CPS/S	K_v VCO GAIN CPS/V	K_D DET GAIN V/DEG.	K_M MULT GAIN	G OPEN LOOP GAIN SEC $^{-1}$	TYPE DC AMPL.	A DC AMPL GAIN	t MAX LOCK-IN TIME MS	ϕ_{ss} Δf MAX DOPPLER ERROR DEG.	ϕ_{ss} $\dot{f}$ MAX ACCEL. ERROR DEG	FILTER TIME CONSTANTS T_1 MS	FILTER TIME CONSTANTS T_2 MS
Main Receiver Loop	(972fo) 2276.4	(928fo) 2173.3	(12fo) 28.104	None	300	82K	3000	300	.00833	81	48,400	Active Filter	50	N/A	±12.2	13.5	605	5
RCVR Acquisition Loop	(12fo) 28.104	(12fo) 28.104	(12fo) 28.104	1/2	500	505	18.5	300	.0833	1/2	4,500	Active Filter	50	.0655	±.81	.03	20.2	3.0
XMTR Tracking Loop	(12fo) 28.104	(12fo) 28.104	(12fo) 28.104	None	1200	2020	37	300	.0933	1	9,000	None	N/A	.0755	± 40.5	.011	7.04	1.25
Med. Fine Range Tone Loop	2.268	2.268	2.268	None	100	84	3.085	120	.025	1	210	Active Filter	100	.23	±.44	.125	23.6	15
Fine Range Tone Loop	(fo) 2.342	(fo) 2.342	(fo) 2.342	None	100	84	3.085	120	.0167	1	720	Active Filter	100	.23	±.42	.125	81	15
RCVR Divide by 24 Loop	(12fo) 28.104	(1/2 fo) 1.171	(1/2 fo) 1.171	None	2000	1010	37	20	.0833	24	14,400	None	N/A	.0041	±25.2	.0038	4.05	0.75
XMTR Divide by 24 Loop	(12fo) 28.104	(1/2 fo) 1.171	(1/2 fo) 1.171	None	2000	2020	37	20	.0833	24	14,400	None	N/A	.016	±25.2	.0038	4.05	0.75
RCVR Synthesizer x58 Multiplier	(1/2 fo) 1.171	(29fo) 67.918	(14.5 fo) 33.959	58	1200	220	44.7	600	.125	1	27,000	None	N/A	.028	± 16.3	.0126	21	1.25
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XMTR Synthesizer x 57 Multiplier	(1/2 fo) 1.171	(28.5 fo) 66.747	(9.5 fo) 22.249	57	1500	1596	29.4	2000	.0833	1	60,000	None	N/A	.0242	± 4.8	.003	.30	1.0
XMTR Synthesizer x 60 Multiplier	(1/2 fo) 1.171	(30fo) 70.260	(30fo) 70.260	120	4000	10,080	183.2	1000	.0333	2	24,000	DC amp	4	.0506	± 18.9	.0046	6.75	0.375
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Spectrum Gen #1 x 6.0 Multiplier	(1/2 fo) 1.171	(3.0fo) 7.0260	(3.0fo) 7.0260	30	2000	2520	46.2	600	.0833	5	90,000	None	N/A	.0254	±5.04	.0047	25.3	0.75
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Spectrum Gen. #2 x 11.8 Multiplier	(1/2 fo) 1.171	(1/2 fo) 13.8178	(5.9fo) 13.8178	59	3000	4960	91	1500	.0416	5	112,500	None	N/A	.0292	±7.94	.0041	14.1	0.50

TABLE 4-1 AROD TRANSPONDER LOOP CHARACTERISTICS

limiter preceding the phase detector results in a signal suppression factor which effectively varies the loop gain as a function of predetection noise-to-signal ratio. Stated mathematically

$$\alpha = \frac{1}{\sqrt{1 + \frac{4}{\pi} \frac{P_N}{P_S}}}$$

and $G = \alpha G_o$

where G_o is the loop gain at $\alpha = 1$.

4.2.2 Range Tone Loops

The calculations for both of the range tone loops were based on the equations described in the preceding section. The resultant data is tabulated in Table 4-1. Both loops were designed for minimum phase error versus Doppler at a 100 cps loop noise bandwidth. The 2.342 mc loop did not use a limiter preceding the phase detector. If a limiter had been used, the detected coarse range tone amplitudes would have varied as a function of noise-to-signal ratio due to the signal suppression factor. Using the linear loop minimizes amplitude changes in the coarse range tones to less than 1 db due to AGC error. The 2.268 mc loop uses a limiter since the coarse range tone detection is not required in this loop.

4.2.3 Tracking Divider and Multiplier Loops

The calculations for all of the remaining loops in the AROD Transponder utilized the equations previously derived. These loops were designed primarily to act as narrow band filters. Loop bandwidths were selected to minimize acquisition time where

$$t_{acq} \approx \frac{4\,\Delta f^2}{B_L{}^3}$$

Results of all the calculations may be found in Table 4-1. In some cases, DC amplifiers were used to increase loop gain to maintain low steady-state errors at maximum Δf.

4.3 AGC Loop Calculations

The AGC loop contains the phase detector and the AGC active loop filter in the AGC Demodulator board and the gain controlled cascode IF amplifier stages in the First and Second IF Amplifiers. When the main receiver phase locked loop is locked on a carrier, the Receiver VCO supplies an essentially noise free signal, which is phase coherent with the carrier, to the reference of the AGC phase detector. The carrier is applied to the other input of the phase detector and the static phase difference between the two signals is adjusted so that the phase detector

becomes a coherent amplitude detector. Thus, a coherent type of AGC system is established which responds only to the amplitude of the received carrier.

For the purpose of this discussion, let the gain controlled stages be referred to as a voltage controlled attenuator (VCA), with a gain constant, K_{VCA} in db/volt. Then the equivalent loop of the AGC system is shown in Figure 4-2.

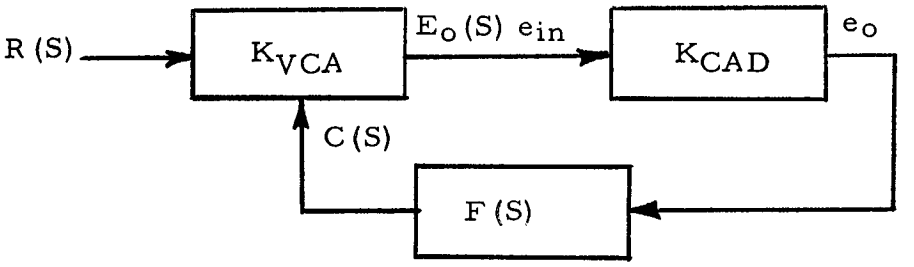


FIGURE 4-2. EQUIVALENT AGC LOOP

where:

K_{VCA} = gain constant of VCA in db/volt.

K_{CAD} = gain constant of coherent amplitude detector in volts/db.

F (S) = filter transfer function.

R (S) = Laplace transform of input function.

The open loop transfer function is:

$$H_o(S) = K_{VCA} K_{CAD} F(S) = G F(S)$$

where

$$G = K_{VCA} K_{CAD}$$

and the closed loop transfer function is:

$$H(S) = \frac{H_o(S)}{1 + H_o(S)} = \frac{G F(S)}{1 + G F(S)}$$

The equivalent circuit of the AGC active loop filter is shown in Figure 4-3 (the input impedance of the DC amplifier is many times greater than R by design and can be neglected). An analysis of this circuit shows that the transfer function is:

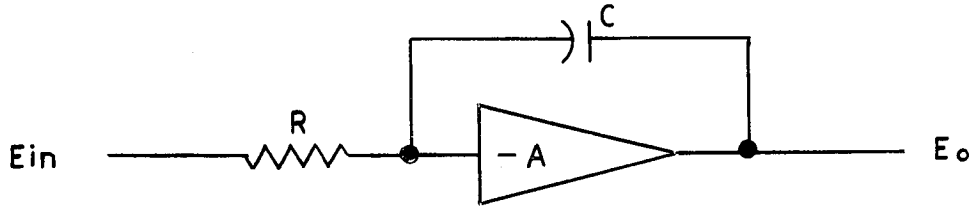


FIGURE 4-3. ACTIVE LOOP FILTER

$$F(S) = \frac{E_o}{E_{in}} = \frac{-A}{1 + RSC + ARSC} = \frac{-1}{\frac{1}{A} + \frac{RSC}{A} + RSC}$$

or, for $RSC \gg \frac{RSC}{A}$

$$F(S) \approx \frac{-1}{\frac{1}{A} + \tau S}$$

where $\tau = RC$

A = DC amplifier gain

Substituting $|F(S)|$ into the equation for $H(S)$ yields:

$$H(S) = \frac{\frac{G}{\frac{1}{A} + \tau S}}{1 + \frac{G}{\frac{1}{A} + \tau S}} = \frac{GA}{1 + GS + A\tau S}$$

or

$$H(S) = \frac{G}{\frac{1}{A} + G + \tau S}$$

for $\frac{1}{A} \ll G$, this reduces to

$$H(S) = \frac{G}{G + \tau S}$$

or

$$H(j\omega) = \frac{G}{G + j\omega\tau}$$

By definition, the one sided loop noise bandwidth is:

$$B_L = \int_0^\infty \left| H(j\omega) \right|^2 d\omega$$

substituting for $H(j\omega)$ into the expression for B_L and performing the integration yields

$$B_L = \frac{G\pi}{2\tau} \quad \text{in radians per second}$$

or

$$B_L = \frac{G}{4\tau} \quad \text{in cycles per second}$$

It can be shown that the steady state error in the AGC loop, due to a step function input of amplitude ΔE_{in}, is:

$$e_{ss} = \lim_{S \to 0} \; S \; 1 - H(S) \; \frac{\Delta E_{in}}{S}$$

$$= \lim_{S \to 0} \; 1 - \frac{GA}{1 + GS + A\tau S} \; \Delta E_{in}$$

$$= \lim_{S \to 0} \; \frac{1 + GA + A\tau s - GA}{1 + GA + A\tau S} \; \Delta E_{in}$$

$$e_{ss} = \frac{\Delta E_{in}}{1 + GA}$$

or, for $GA \gg 1$

$$e_{ss} = \frac{\Delta E_{in}}{A \, K_{VCA} \, K_{CAD}}$$

The gain constant of the CAD is:

$$K_{CAD} = .115\, E_o \quad \frac{\text{volts}}{\text{db}}$$

where E_o = peak of the CAD "S" curve for $\phi = 0$

For the following system design parameters, the AGC loop performance can be predicted:

E_{in} = 20 db (100 to 1000 Nautical Miles)

E_o = 1.0 volts

τ = .11 sec

$$K_{VCA} = \frac{20 \text{ db}}{\text{volt}}$$

A = 50

and

$$B_L = \frac{20 \times .115}{4 \times .11} = 5.2 \text{ cps}$$

$$e_{ss} = \frac{20}{(50)\,(2.3)} = .174 \text{ db}$$

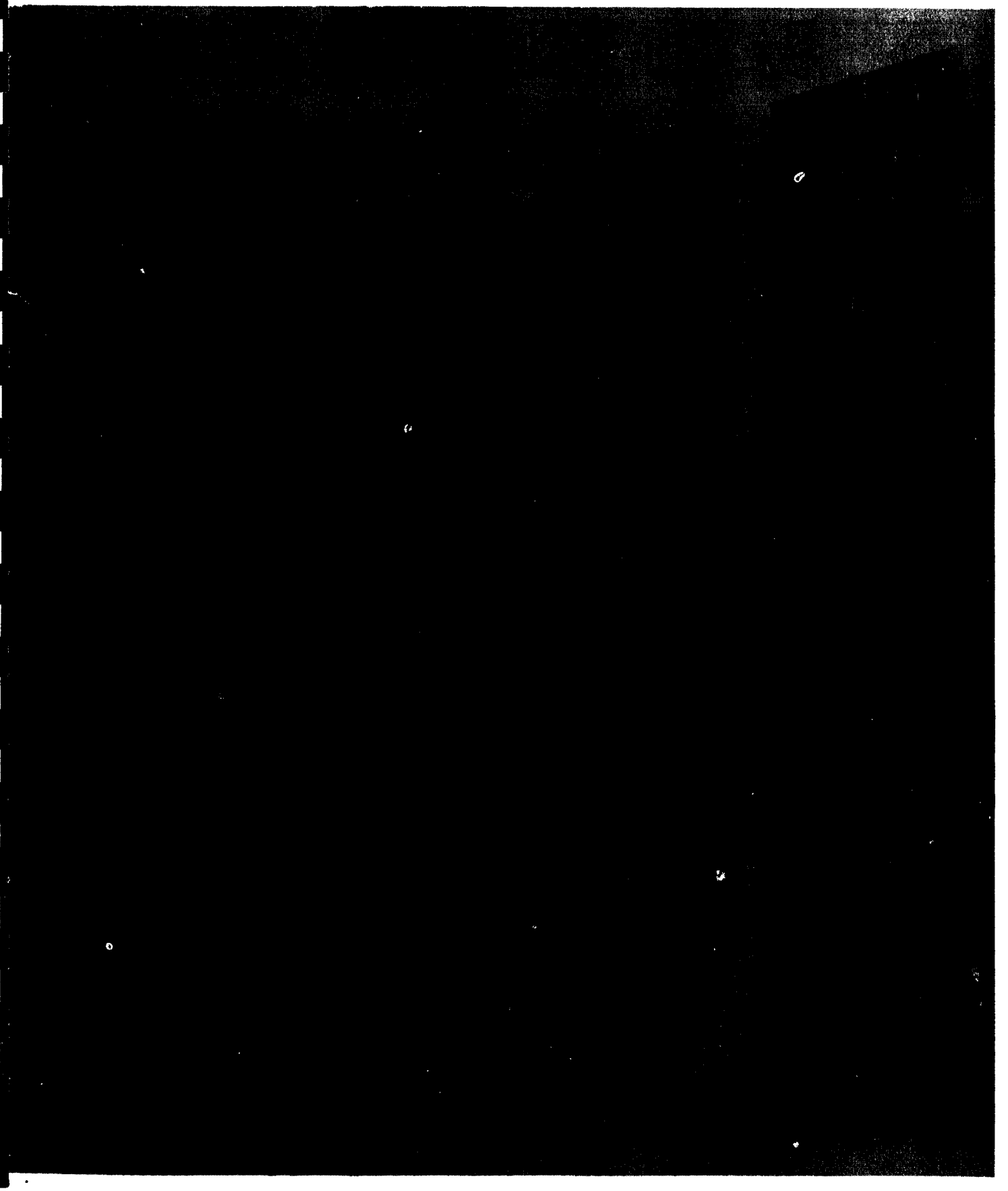
For the design goal of 50 db dynamic range:

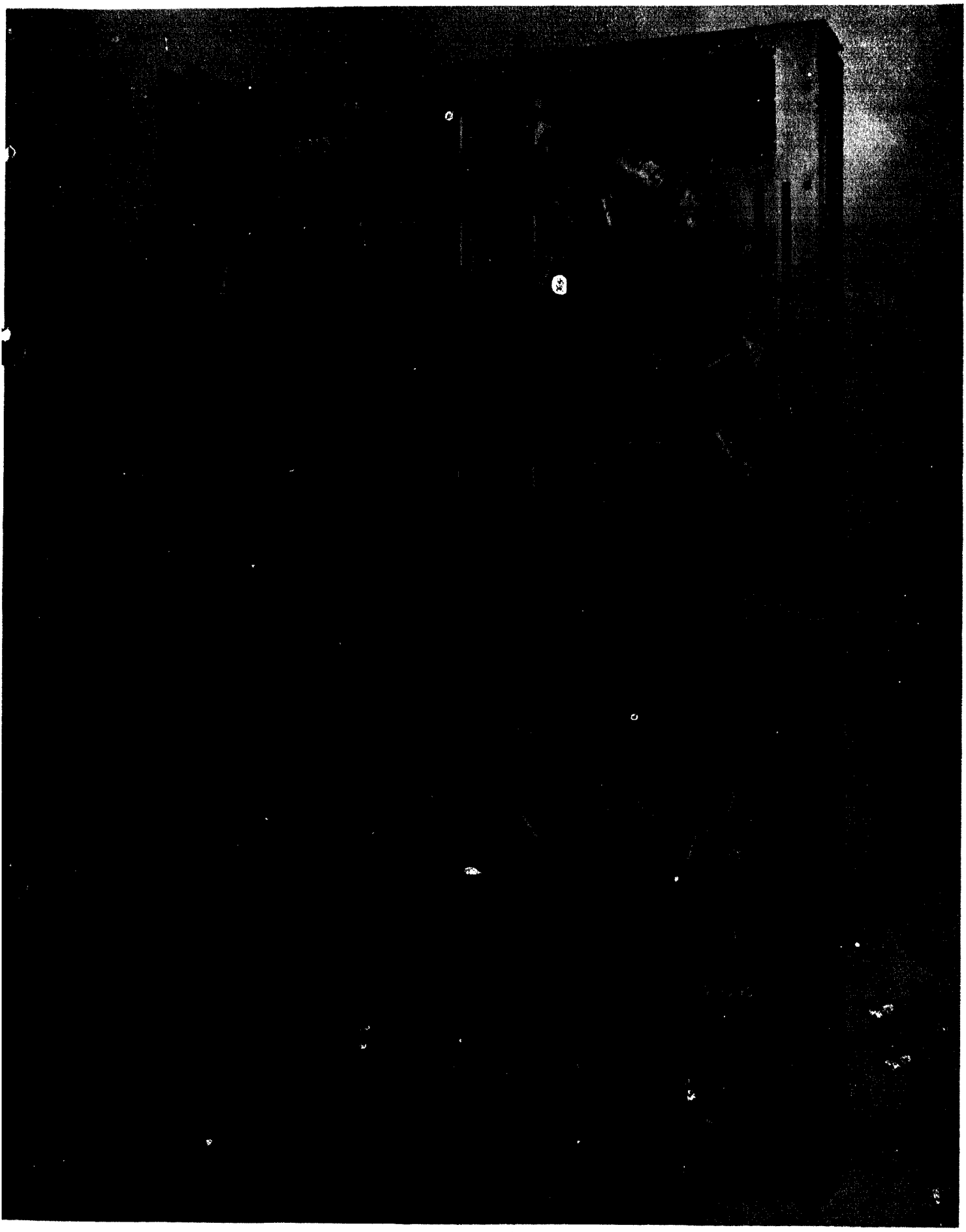
$$e_{ss} = \frac{50}{(50)(2.3)} = .435 \text{ db}$$

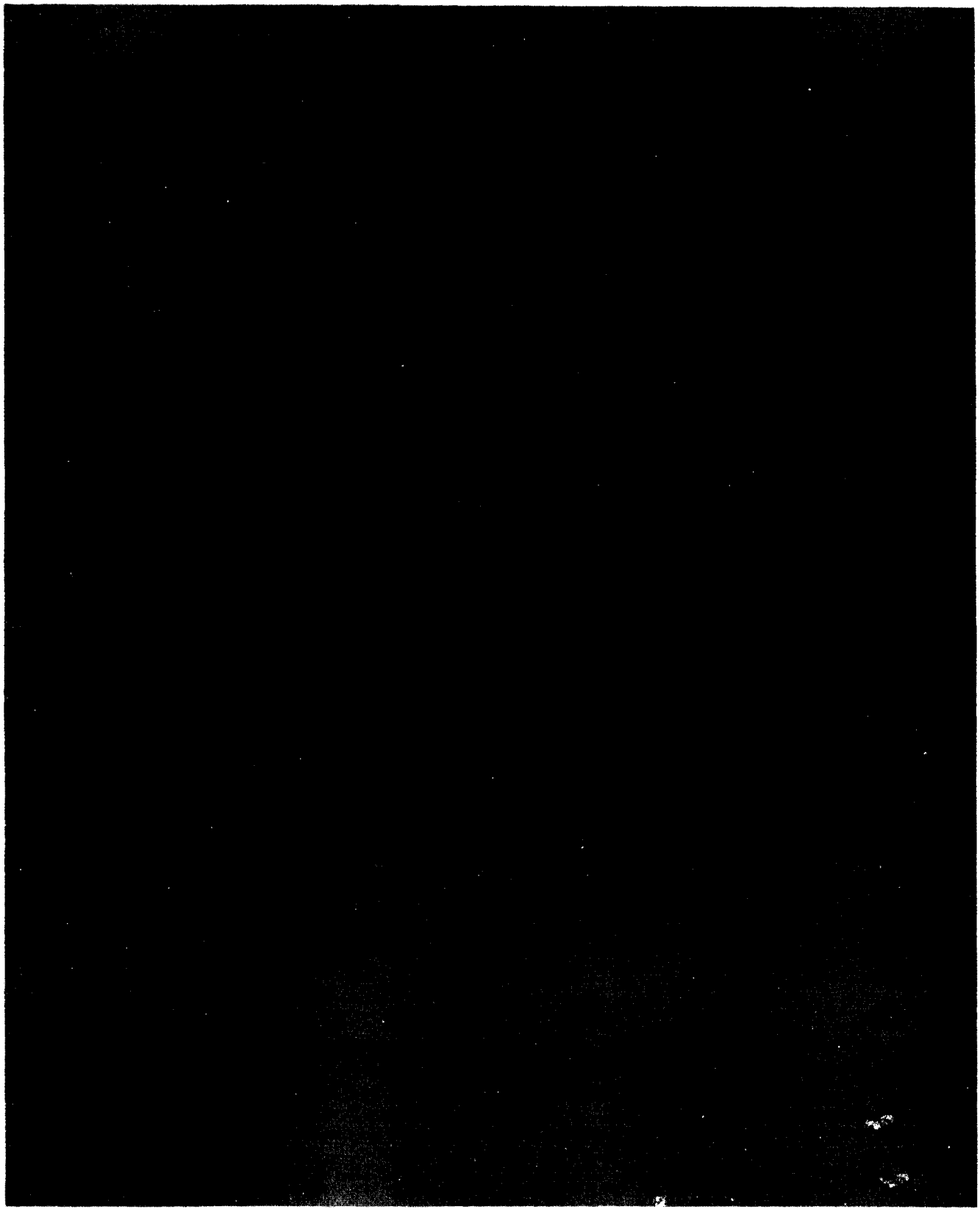
4.4 Packaging

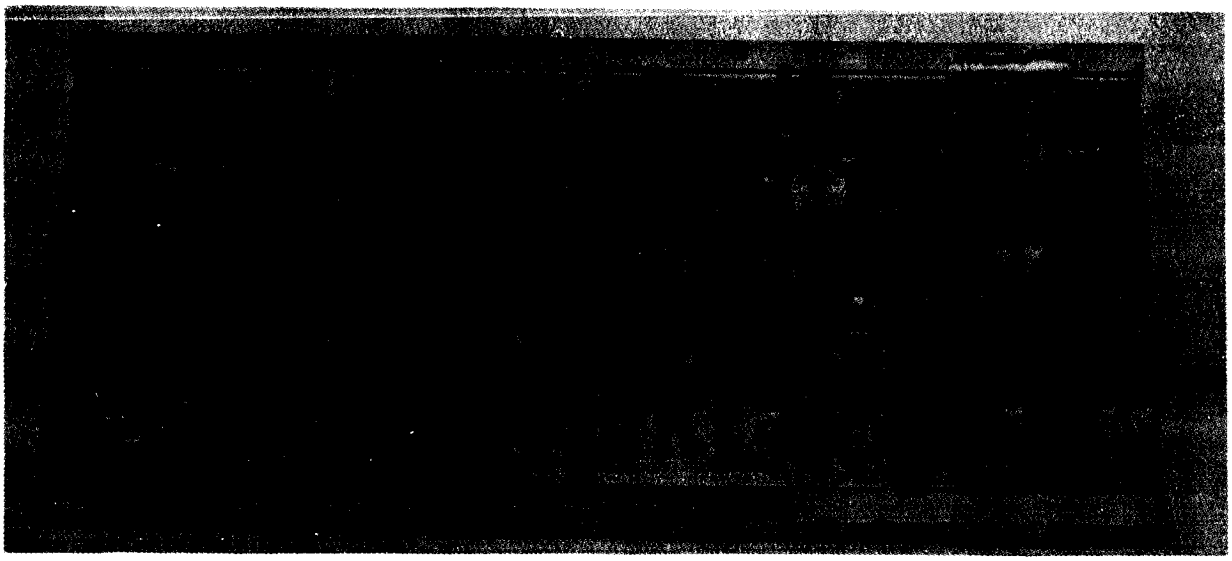
The packaging scheme was selected to provide maximum RFI shielding, maximum versatility for incorporation of future changes with minimum redesign effort, and an easily reproduced method of circuit construction for most economical production in large quantities. Ordinary printed circuit techniques were used for low-frequency and/or non-critical circuits. Improved shielding and isolation of RF and IF circuits was provided when necessary by use of transformers enclosed in gold-plated shield cans. For higher-frequency and/or more critical circuits, a double-sided printed circuit board was used. This technique allowed better isolation and shielding and reduced the common-ground lead inductances at the higher frequencies. The double-clad boards were not used in the first unit due to the delivery schedule but were found to be so successful that several boards were redesigned for use in the second unit.

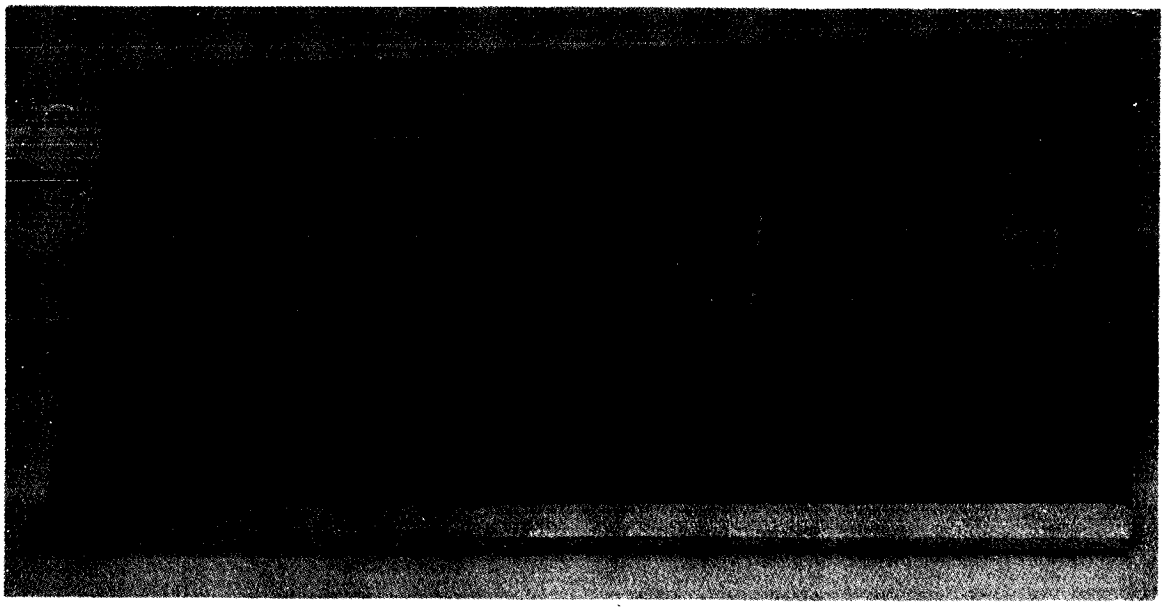
The overall packaging scheme, a typical module, and typical printed circuit boards are illustrated in the following photographs.











SECTION V

DISCUSSION OF CIRCUIT DESIGN

V. DISCUSSION OF CIRCUIT DESIGN

5.1 Receiver

5.1.1 First and Second IF Amplifier

The function of the First and Second IF Amplifier is to:

1. Establish an IF amplifier noise figure of 7.0 db or less.

2. Provide sufficient gain to the carrier and sideband signals from the first mixer such that the required gains of succeeding amplifiers does not become impractical.

3. Present a 50 ohm resistive load to the microwave mixer.

4. Provide 50 db of automatic gain control.

5. Down convert the 103.048 mc first IF to 14.052 mc.

6. Accomplish the above functions within a signal bandwidth sufficiently large that any phase shift introduced on the fine range tone sidebands are

negligible at the maximum Doppler offset.

The First IF Amplifier contains, in the signal path:

1. An input matching network to establish the 50 ohm resistive input impedance.

2. Two broadband, double-tuned, neutralized amplifiers.

3. A broadband cascode amplifier for AGC control.

4. A double-balanced mixer.

In addition, a broadband neutralized amplifier tuned to 88.996 mc, the 2nd mixer reference frequency, is provided for isolation in the injection signal path of the 2nd mixer. An impedance matching network at the input of this stage establishes a resistive input impedance of 50 ohms.

The Second IF Amplifier consists of two broadband, cascode amplifiers tuned to 14.052 megacycles. AGC control is applied to both of these stages in addition to the cascode stage in the First IF Amplifier.

The principle of the neutralization method used is

illustrated in the simplified equivalent circuit of Figure 5-1. The input signal is applied between the emitter and base of the transistor by the secondary winding of the balanced transformer T_1, and the amplifier output appears

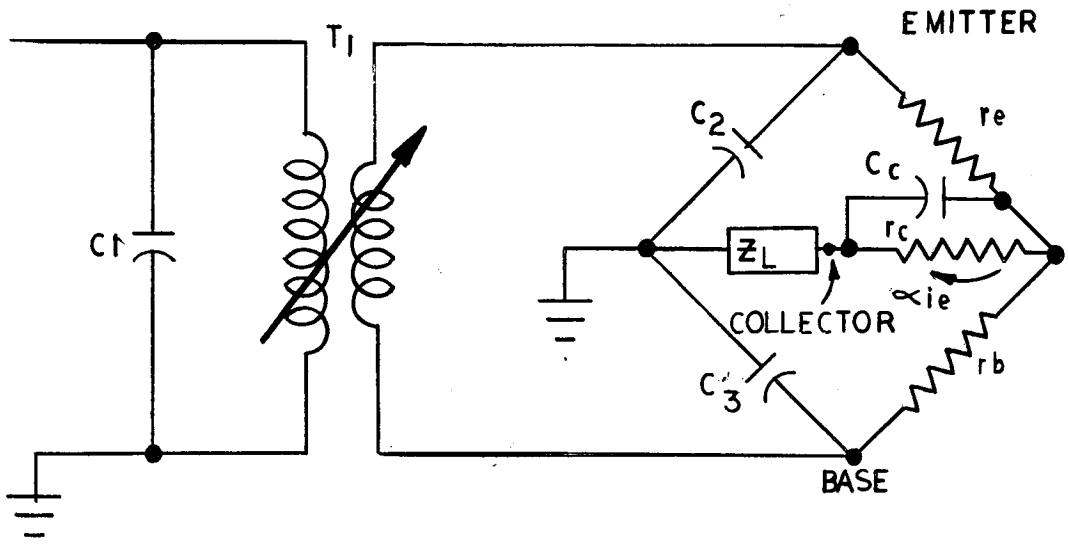


FIGURE 5-1. TRANSISTOR NEUTRALIZATION BRIDGE NETWORK

across Z_L in the collector circuit. Internal feedback from the collector to the junction of r_e and r_b through the parallel combination of r_c and C_c is balanced, or nulled, at the emitter to base terminals if:

$$1.\quad \frac{\frac{1}{SC_2}}{r_e + \frac{1}{SC_2}} = \frac{\frac{1}{SC_3}}{r_b + \frac{1}{SC_3}}$$

or by simplifying

$$2.\quad \frac{1}{SC_2\, r_e + 1} = \frac{1}{SC_3\, r_b + 1}$$

or

$$3. \quad SC_2 r_e + 1 = SC_3 r_b + 1$$

and finally

$$4. \quad SC_2 r_e = SC_3 r_b$$

From equation (4), it is evident that if the capacitive reactances of C_2 and C_3 are properly chosen, i.e., if:

$$5. \quad \frac{SC_2}{SC_3} = \frac{r_b}{r_e}$$

then internal feedback through the transistor is balanced out and that, furthermore, the resulting neutralization bridge is frequency insensitive. Reverse voltage gains as high as -40 db have been obtained with this type of neutralization. This circuit requires a balanced input since neither the base nor the emitter may be grounded; however, this is not a penalizing requirement. By the proper choice of components, the network shown can be used as a single tuned impedance matching input network, as a single tuned transformer coupled interstage network, or as a double tuned equivalent of either of the above. In the 103.048 megacycle stages of the First IF Amplifier, the input and the interstage transformers are designed for double-tuned, transitional-coupling for maximum gain-bandwidth.

The problem of providing automatic gain control for tuned IF amplifiers, without degrading the bandpass characteristics of the amplifier, is well known. This problem was given careful attention in the selection of the AGC method of the AROD Transponder Receiver. The severe requirement of negligible phase shifts on the fine range tone sidebands dictate that a minimum number of tuned circuits be used in the sideband signal path and that these circuits have the widest practical bandwidth; and the AGC action must have the minimum possible effect on the center frequency and bandwidth of any tuned circuits in the gain controlled stages. The first requirement indicated that active AGC stages which have power gain, as opposed to voltage controlled attenuators with inherent insertion losses, were desired. A review of the effects of transistor parameter changes upon the Q and center frequency of tuned circuits, with either forward or reverse AGC, indicated the need for isolating the tuned circuits from the gain controlled stage. A cascode circuit, which satisfies both of the above requirements, was used as the AGC'd stages in the first and second IF amplifier. A typical circuit consists of transistors Q3, Q4 and Q5 in SCI Drawing 362069. In this circuit, the gain of the grounded emitter stage is controlled by using the relationship of the current gain β to the emitter bias current. The bias current is varied by means of the variable voltage divider consisting of R13, R14 and transistor Q3.

The effectiveness of the cascode arrangement can be appreciated when it is realized that the tuned circuit of this stage is isolated from changes in transistor parameters as Q4 bias is changed. The operating point of Q5 is not varied and any change in the output impedance of Q4 is isolated from the tuned circuit by the grounded base amplifier, Q5. The interstage bandwidth between Q4 and Q5 is sufficiently large, due to the low input impedance of the grounded base stage, that the effects of collector impedance changes of Q4 are insignificant. Changes in the input impedance of a grounded emitter amplifier with changes in the emitter bias are not severe. This, in addition to the small damping resistor, R11, across the secondary of the input transformer, effectively isolates the controlled stage from the tuned circuit of the preceeding stage. AGC compressions of 20db per stage with very small effect upon the overall bandpass characteristics are obtainable with this circuit.

The second mixer, consisting of transistors Q7 and Q8 in SCI Drawing 362069, is a double-balanced configuration in which both input signals are balanced out at the common collector circuit, leaving only the beat signals and harmonics of the inputs. In this circuit, the single ended IF input is applied to both the base of one transistor and to the emitter of the other, and the

single ended reference signal is applied to the other base-emitter pair. Since the voltage gain of the grounded emitter stage is equal and opposite to that of the grounded base stage, the net gain is zero at the input frequencies. The only additional balancing necessary for this type of circuit is a balancing of the transistor gains; however, balancing requirements are not critical in this application and additional balancing controls were not included. The bandwidth of the tuned circuit in the collector circuit (approximately 20 mc) is sufficiently wide to avoid phase shift problems on the fine range tone sidebands, yet it effectively filters out harmonics of either mixer input. The injection signal level was adjusted, by the voltage divider of R27 and R28, for the best S/N ratio from the mixer.

5.1.2 Sideband and Carrier IF Amplifiers

The functions of the Sideband and Carrier I.F. Amplifiers are:

1. To separate the carrier from the range tone sidebands, thereby forming separate channels for each of these signals to the product demodulator in the Sideband Demodulator Board.

2. To reduce the noise bandwidth through the sideband channel to approximately 60 kilocycles.

3. To reduce the noise bandwidth through the carrier channel to approximately 17 kilocycles.

4. To provide amplification to the range tone sidebands and to the carrier.

5. To accomplish the above functions in a manner which will preserve the required phase relationships of the range tone sidebands and the phase relationship of the sidebands to the carrier. The requirement that the phase slopes of each crystal filter be inversely proportional to its center frequency has been established in a previous section of this report.

6. To provide an analog monitor output proportional to the S/N ratio in the carrier channel.

Specifications for the proportional phase slope crystal filters, as written by Space Craft, Inc. for the vendor, are listed below:

Specifications Item I - AROD Proportional Slope IF Sideband Filters

1. Z = 50 ohms ± 5% resistive source and load.

2. Phase slopes inversely proportional to filter center frequency.

3. Temperature range -22°C to +70°C.

4. Differential phase shift on highest modulation frequency (2.342 mc) due to all causes (±36 ppm Doppler, temperature, and other causes) to be ±0.5 degrees maximum, design goal.

5. Differential phase shift on other modulation frequencies from all causes ±2 degrees maximum.

6. Noise bandwidth on Filter #1 to be 15 KC maximum. Noise bandwidth on other filters to be somewhat greater in approximate proportion to center frequency. (Input noise bandwidth approximately 10 mc).

7. Approximate physical size $2\frac{1}{2}$ x $3\frac{1}{4}$ x 1 for 4 each filters in each package.

8. Input and output connector Microdot Type 31-01 (Mating Microdot Connector is 32-23).

9. Overall insertion loss 12 db maximum. Insertion loss on Fb, F3, F1, and Fa to be matched within ±0.5 db.

10. Maximum relative attenuation between F1 and F1 ± Δf and F2 and F2 ± Δf to be 1 db maximum. (Δ f to include ±36 ppm Doppler, temperature effects, etc.)

11. Shock and Vibration: Normal bench handling.

12. Ultimate Rejection: 30 db minimum at 73 kc from center frequency.

Specifications Item 2 - AROD Carrier Filter

1. Center frequency 14.052 mc (tolerance on center frequency to be determined by phase considerations, Item 10).

2. Noise bandwidth approximately 15 kc maximum.

3. Temperature: -20°C to 70°C.

4. Approximate physical size, $2\frac{1}{4}$ x 1 x 1.

5. Input and output connector Microdot 31-01 (Mating Connector is Microdot 32-23).

6. Insertion loss 3 db maximum.

7. Source and load Z = 50 ohms ±5% resistive.

8. Ultimate rejection 40 db at 100 kc maximum.

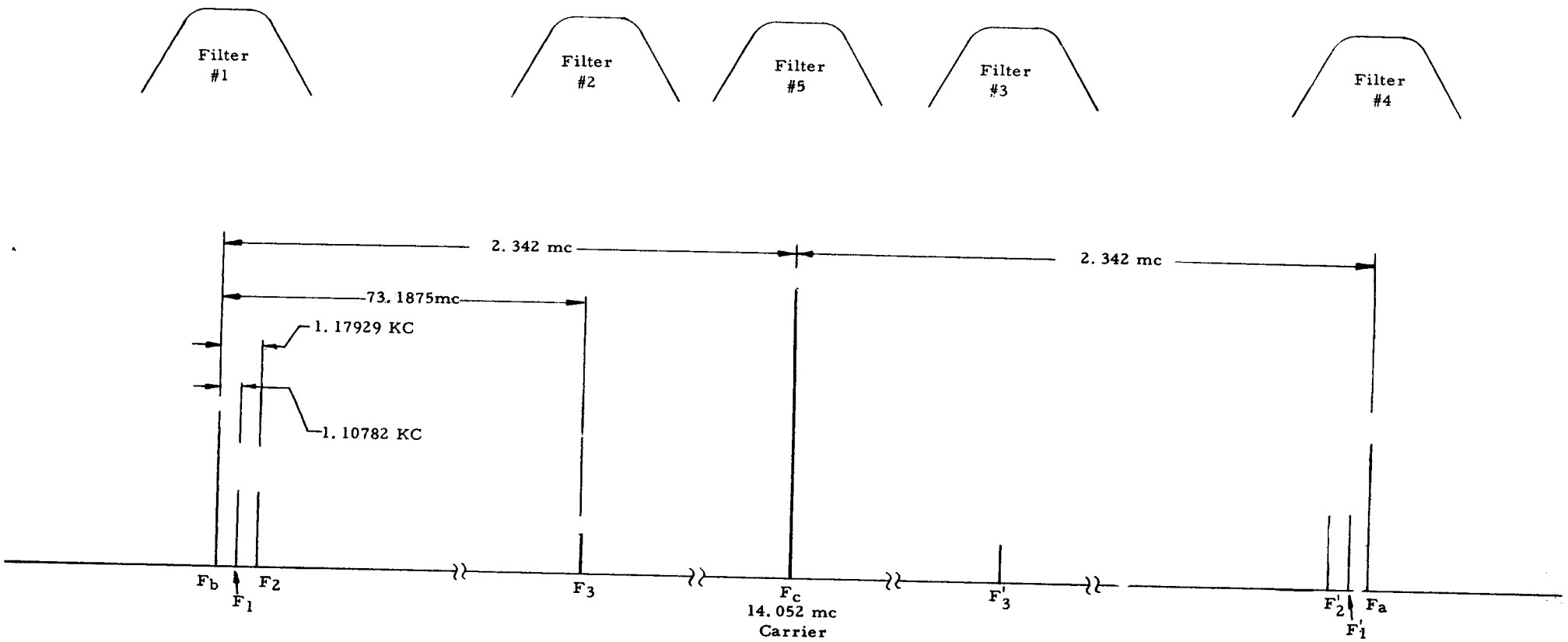
9. Shock and Vibration: Normal bench handling.

10. Phase slope inversely proportional to frequency referenced to sideband filter #1, Figure 5-2, phase error to be less than $\pm 5^{o}$ due to all causes (±36 ppm Doppler, temperature and other causes).

The Sideband I. F. Amplifier schematic is shown in SCI Drawing 362100. Transistor stages Q1, Q2, Q3, and Q4 are single-tuned, wide-band amplifiers with approximately 15 db gain each; the interstage bandwidths are approximately 30 megacycles. Neutralization was not necessary for these amplifiers because of the relatively low gain per stage.

An output to the Carrier I. F. Amplifier is provided from the secondary of transformer T1. A 50 ohm attenuation pad, consisting of resistors R5, R6 and R7, provides approximately 10 db of isolation between the input of the Carrier I. F. Amplifier and the input circuit of transistor Q2.

To insure proper performance of the crystal filters,



$F_c - F_b = 2.342$ mc
$F_1 - F_b = 1.1078$ KC
$F_2 - F_b = 1.17929$ KC
$F_3 - F_b = 73.1875$ KC

$F_c = 14.052$ mc
$F_b = 11.710$ mc
$F_a = 16.394$ mc
$F_3 = 11.7831875$ mc
$F'_3 = 16.3208$ mc

Doppler = ±36 ppm

Filter Phase Slopes to be Inversely Proportional to Frequency

FIGURE 5-2. PROPORTIONAL PHASE SLOPE FILTER REQUIREMENTS

the correct terminations at both the input and output of the filter must be provided. The importance of providing the correct terminations at these points can be realized when it is noted that the center frequencies of the two fine range tone filters are 4.684 megacycles apart and each of the filters must be properly terminated. According to the filter vendor, a proper termination consists of a 50 ohm resistive source and load, each shunted by a total of 12 picofarads. The filter output termination consists of variable capacitor C18 and the 50 ohm, 10 db attenuation pad formed by resistors R15, R16 and R17. The input termination is provided by the transistor buffer stage, Q5, which has as its load impedance a 51 ohm resistance, R12, shunted by variable capacitor C15. The proper input and output reactances were adjusted with an R-X meter, through a half wavelength coaxial cable at 14.052 megacycles.

The schematic of the Carrier I.F. Amplifier is shown in SCI Drawing 362105. Transformer T2 and capacitors C1, C2 and C3 were selected to provide a resistive input impedance of 50 ohms. Amplifier Q2 provides approximately 20 db of gain to the entire spectrum of signals from the Sideband I.F. Amplifier, and applies them to the carrier filter. The filter bandwidth is sufficiently narrow to pass only the carrier signal to amplifier Q3 for an additional 20 db of amplification. Amplifier Q3 then feeds the

carrier to the demodulator boards. Amplifiers Q2 and Q3 are neutralized (see the circuit description of the First I. F. Amplifier for an explanation of the method of neutralization), single-tuned I. F. stages. The requirements for the carrier filter terminations are the same as for the sideband filters except that the bandwidth requirements are not nearly as severe. The termination networks consist of the 50 ohm attenuation pads of R9, R10 and R11 at the input and R12, R13 and R36 at the filter output. Each pad provides an isolation of 10 db between the filter and the transistor circuits. Capacitors C14 and C15 were selected to provide a capacitive reactance equal to 12 picofarads at the filter input and output networks.

The function of the circuits which include transistors Q4, Q5 and Q6 is to provide an analog monitor output which is proportional to the S/N ratio in the carrier channel. For a better understanding of the significance of this circuit, refer also to the AROD Transponder Receiver Block Diagram, SCI Drawing 362034; the S/N monitor circuit includes the last six blocks of the Carrier I. F. Amplifier. Note that the total gain from the 1st mixer to the output of the first stage of the Carrier I. F. Amplifier is sufficient to produce a relatively large noise level within the wide overall bandwidth up to this point. If a signal is also present in the amplifiers,

a large part of the noise power appears as AM modulation impressed on the signal. After approximately 20 db of amplification at the IF frequency by amplifier Q4, the AM noise components are removed from the carrier by the detector CR1. The low pass, M-derived filter consisting of C43, C44, and C45 and L8 has a notch at 14.052 megacycles so that only low frequency noise components are applied to the noise amplifier Q6. The noise is amplified by Q6 and rectified by the transistor noise detector Q5; the AC components are removed by the low pass filter consisting of R40 and R34 in the Q5 collector circuit. The amplifier gains were selected such that the inherent system noise, in the absence of any signals, will just saturate Q5; therefore, the DC voltage level at monitor point 10A will be approximately 1.0 volt. Now, consider the case where the receiver is locked on a signal. The AGC loop will hold the total power (signal plus noise) into the S/N monitor circuit approximately constant; i.e., as the signal level increases, the noise level will decrease. As the noise level decreases, the drive to the noise detector decreases and the DC level at monitor point 10A increases to approximately 20 volts at the maximum signal level specified for the AROD Transponder Receiver. Thus, it is seen that the DC level at the monitor point is a function of the S/N ratio present in the Carrier I.F. Channel.

5.1.3 Demodulators

This module contains the Sideband Demodulator board, the Carrier Demodulator board and the AGC Demodulator board.

5.1.3.1 Sideband Demodulator

The Sideband Demodulator schematic is shown in SCI Drawing 362075. In the sideband signal path is the isolation amplifier Q1, the product detector consisting of Q2 and Q3, and the buffer amplifier Q4.

Amplifier Q1 is a single tuned, grounded emitter I. F. stage tuned to 14.052 megacycles. It provides approximately 15 db gain to the sideband signals in an interstage bandwidth of approximately 25 megacycles.

The product detector is similar to the double balanced mixer described in the First I. F. Amplifier section. The 14.052 megacycle injection signal, which is derived from the Receiver VCO, is applied to the base of Q3 and to the emitter of Q2. Because the gain of the grounded base stage is equal and opposite to the gain of the grounded emitter stage, the injection signal is balanced out in the collector circuit. Likewise, the sideband I. F. signals are balanced at the collector leaving only the products and even order

harmonics of the carrier and sidebands. The 2.342 megacycle bandpass filter, consisting of L11 and C53 and C54 at the collector circuit, ensures that only the demodulated range tones will be presented to the Range Tone Circuit.

The video amplifier and detector Q5 and CR4 provide a DC output to the monitor panel which is proportional to the total demodulated signal power output of the product demodulator.

The 28.104 megacycle signal from the Receiver VCO is applied to the varicap divide-by-two circuit by the driver amplifier stage, Q6. The resulting 14.052 megacycle signal is distributed by amplifiers Q7, Q8, and Q9 to supply the reference signal for the product demodulator, the carrier phase detector and the AGC phase detector respectively. The I.F. stages of Q6, Q7, Q8 and Q9 are identical to the neutralized I.F. amplifiers discussed in previous sections except for center frequency. Attenuation pads at the output of Q7 sets the proper signal level to each reference output.

In the divide-by-two circuit, which includes varicaps CR1 and CR3, the primary winding of transformer T5 was designed to form a series resonant circuit with the two varicaps at the desired output frequency at 14.052 megacycles; resistor R29 and the turns ratio of T5 were selected to allow the maximum practical Q

of this circuit. Diode CR2 limits the back bias on the varicaps to facilitate proper tuning and to increase the circuit's tolerance to changes in drive level.

5.1.3.2 Carrier Demodulator

The schematic of the Carrier Demodulator is shown in SCI Drawing 362085. This board contains the phase error detector of the Transponder Receiver's main phase locked carrier loop. The 14.052 megacycle carrier is applied to one input of the phase detector, via transistors Q1 and Q5 and the 14.052 megacycle reference signal derived from the Receiver VCO is applied to the other input via transistor Q4. The phase detector output, which is proportional in amplitude and polarity to the difference in phase of these two signals, is applied to the Receiver VCO (through the Main Loop Filter) to close the loop.

In the acquisition mode, the Receiver VCO must be locked on a 28.104 megacycle signal from the Command Receiver. Accordingly, the Command Receiver output is amplified by Q3, divided to 14.052 megacycles by the divide-by-two circuit of CR5 and CR6, and is then applied to the signal input side of the phase detector by transistors Q2 and Q5. Transistor Q1 is switched off during the acquisition mode and transistors Q2 and Q3 are switched

off after acquisition is completed in order that both the carrier and Command Receiver output are never simultaneously applied to the phase detector.

Transistor stages Q1, Q3, Q4 and Q5 are neutralized I. F. amplifiers; the method of neutralization has been explained in Section 5. 1. 1. Transistor stage Q2 is a grounded emitter configuration in order that an output to the AGC Demodulator board be provided for acquisition purposes. This will be explained in the next section. Transformers T1, T5, T6 and T10 are designed to provide a 50 ohm resistive impedance at their respective inputs.

Diodes CR3 and CR4 form a shunt limiting network in the collector circuits of Q1 and Q2. The basic purpose of the limiter is to reduce the noise spikes from the system in order that the reference level requirements into the phase detector did not become impractical. This method permits the use of a larger S curve for increased open loop gain with minimum degradation in the carrier S/N ratio.

The phase detector, which includes CR9 and CR10, is a standard two-diode peak detector operating with the coherent inputs normally in quadrature. The detector is designed to oper-

ate with a reference input level greater than twice the signal input level. The reference input is link coupled to the detector to reduce discriminator action unbalances due to Doppler. A differential capacitor is used between each side of the reference input transformer to balance any reactive components inherent in the circuitry. The S curve of the detector is approximately 5 volts peak with a -20 dbm carrier input to this board.

The divide-by-two circuit has been explained in the previous section, 5.1.3.1.

The switching circuits operate as follows:

When the Transponder Receiver main loop is locked, the Schmitt trigger output is approximately +19 volts DC. This voltage is applied to the transistor gate Q6, through the voltage divider of R34 and R2. The divider is designed to supply sufficient voltage to saturate Q6 so that its collector impedance is small. Note that the emitter resistor of Q1 (also the emitter resistor of Q1 in the AGC Demodulator board) is grounded through Q6 and CR1 when Q6 is saturated; therefore, Q1 is biased on and amplifying. The voltage at Q6 collector is approximately +0.5 volts or less. The voltage divider consisting of R16 and CR8 applies approximately -0.7 volts to the cathode of CR2 and to the base bias

network of transistors Q2 and Q3 in the Command-Receiver signal path, so that these two stages are biased off.

When the receiver is in the acquisition mode, there is no output from the Schmitt trigger, and transistor Q6 is off; the voltage at Q6 collector is approximately +15 VDC. Diode CR1 is reverse biased so that transistor Q1 cannot conduct but CR2 is now forward biased. Current flows through R5 and CR2 to establish proper base bias voltages at transistors Q2 and Q3. These transistors are biased on and the signal path between the Command-Receiver input and the phase detector is completed.

5.1.3.3 AGC Demodulator

A brief discussion of the AGC system is included in the Receiver section of the AROD Transponder Theory of Operation. For a detailed schematic of the AGC Demodulator, refer to SCI Drawing 362108.

Transistor Q1 stage is a switched, distribution amplifier tuned to 14.052 megacycles. The input impedance of Q1, through transformer T1, is 50 ohms resistive. Q1 receives the carrier from the Carrier I.F. Amplifier and distributes it to the Carrier Demodulator board and to the AGC product detector. It is switched off dur-

ing acquisition by the output of the transistor gate on the Carrier Demodulator board; for an explanation of the transistor gate and switching circuits, see the section on the Carrier Demodulator. The attenuation pad, consisting of R5, R53 and R54, in the secondary circuit of transformer T2 provides isolation between the Carrier Demodulator input and the input circuit of Transistor Q2. It also provides a gain adjustment in the carrier signal path into the AGC product detector.

Transistor stages Q2 and Q3 are driver amplifiers for the AGC product detector. They are neutralized I. F. stages tuned to 14. 052 megacycles; the method of neutralization has been discussed in the section on the First I. F. Amplifier. The output of the phase detector reference driver, Q3, is link-coupled into the detector to reduce discriminator effects which would produce DC errors due to Doppler shifts.

The product detector, which includes CR1 and CR2, is identical to the phase detector explained in the previous section on the Carrier Demodulator. The S curve is 5 volts peak for a -30 dbm carrier level into the AGC Demodulator board.

Transistor stage Q4 is an isolation I. F. amplifier stage tuned to 14. 052 megacycles. It is neutralized by the bridge neutra-

lization method explained previously. Its input impedance, through transformer T9, is 50 ohms resistive.

The output of Q4 drives the 90 degree phase shifter consisting of the secondary of transformer T8, capacitors C33 and C34 and inductor L4. The input impedance of Transformer T7 is 50 ohms resistive; the inductive reactance of L4 and the capacitive reactance of the parallel combination of C33 and C34 are also 50 ohms at the carrier frequency. The voltages at each end of the T8 secondary are equal in amplitude but 180 degrees out of phase. By superposition, the voltage across the 50 ohm resistive input to T7 lags the voltage of T8 to which inductor L4 is connected by 45 degrees; likewise it leads the voltage of T8 to which the capacitors are connected by 45 degrees. When these voltages are added vectorially, the resultant voltage has been shifted by in phase by 90 degrees from the input voltage.

The AGC active loop filter consists of R22 and capacitor C52 which is connected in parallel with the DC operational amplifier. The operational amplifier provides a DC gain of 50 in the AGC feedback path and acts as a capacitive multiplier in the loop filter. The filter parameters are chosen to establish an AGC loop bandwidth of approximately 3 cycles per second.

The amplifier is a differential balanced type with input and output voltages nominally centered at zero. Temperature stability is obtained by use of the matched input transistors, by the use of a large amount of negative feedback and by the use of compensating transistors Q10 and Q11. Q9 and its associated circuitry form a current source which improves stability by establishing a high degree of coupling between the two differential amplifier sections.

Transistors Q15 and Q16, and the associated circuitry, at the output of the AGC loop filter form a modified Schmitt trigger. The output voltage of the trigger is zero for AGC voltages less than approximately 1.2 volts; it is approximately 19 volts for AGC voltages above this level. The Schmitt trigger drives the transistor gate in the Carrier Demodulator board and the relay, which switches the main loop active filter time constant, on the Main Loop Filter board.

During the acquisition mode, part of the signal from the Command Receiver is applied to transistor Q2 through a 14.052 megacycle half wavelength, lumped-constant, transmission line consisting of L12, C56 and C57. The delay line shifts the phase of the signal so that an AGC voltage of sufficient amplitude to actuate the Schmitt trigger is developed. The Schmitt trigger output causes the Trans-

capacitor C9 is adjusted for maximum output when Q1 is operated as an amplifier at 28.104 mc. Buffer amplifier Q2 isolates the VCXO from load variations so that the required center frequency will be maintained.

The four-stage distribution amplifier feeds the 28.104 mc signal from the VCXO to various other parts of the Transponder as required. One of the amplifiers is gated off to turn off the 28.104 mc signal to the Transmitter Tracking Loop during acquisition.

The Main Loop Filter consists of a high-gain (A = 50) operational amplifier with suitable feedback networks and relay switching to provide the required loop filter and gain characteristics in both the acquisition and operate modes of operation. The feedback network consists of C9, R17, and R4 in the acquisition mode. In operate mode, a 20 db attenuator consisting of R1 and R2 reduces the effective phase detector gain constant to the required value. The feedback network for operate mode consists of C9, R17 and R3. A switching signal from the loop lock sensor in the AGC Demodulator closes the relay as soon as the VCO is locked to the acquisition signal.

ponder Receiver to switch from the acquisition mode over to main loop operation. Then, as long as the receiver is locked on a carrier, an AGC voltage is developed which holds the Schmitt trigger on and the receiver remains in the main loop mode.

5.1.4 Receiver VCO

The Receiver VCO Module contains the 28.104 mc VCXO (SCI Drawing 362180), a distribution amplifier board (SCI Drawing 362031), and the Main Loop Active Filter (SCI Drawing 362082).

The VCXO consists of transistor Q1, a third overtone 28.104 mc crystal and two PC 115 varicaps in the feedback loop to allow frequency control from an external DC control voltage. The two varicaps and coil L2 form a series resonant circuit at approximately the crystal frequency. Pulling of the crystal frequency occurs as a result of the reactive component presented by the series resonant circuit when it is detuned slightly due to DC applied to the varicaps. Coil L3 tunes out crystal holder capacity and serves as a linearity control on the VCXO output frequency—voltage characteristic. Variable resistor R2 sets the DC bias on the varicaps and thus sets the VCXO center frequency to the exact required value. Oscillator tank tuning

5.1.5 Receiver Synthesizer

The Divide-By-24-Loop is shown in SCI Drawing 362009. The loop is designed to provide an output both frequency and phase coherent with the input at 1/24 the input frequency. The loop parameters of gain and bandwidth were selected for minimum phase error versus Doppler, minimum lock-in time, maximum harmonic rejection, and a lock-in range consistent with system requirements.

All of the amplifiers are used for both signal amplification and isolation. Each uses common emitter circuitry operated class A. The collector circuits are single tuned, parallel resonant at the appropriate frequency.

The phase detector used in the divider is a standard two-diode peak detector operating with the coherent input signals normally in quadrature. The detector is designed to operate with a reference input level greater than twice the signal input level. (Reference input refers to the multiplier input—see schematic diagram.) The reference input is link coupled to the detector to reduce discriminator action unbalances due to Doppler. A differential capacitor is used between each side of the reference input transformer to balance any reactive components inherent in the

circuitry. The S-curve of the detector is 5 volts peak resulting in a gain of 0.0833 volts/degree.

The loop filter following the phase detector is a simple RC lead-lag filter. The two time constants set the loop noise bandwidth at a damping factor of 0.71.

The voltage-controlled oscillator (VCO) used in the divider operates at exactly 1/24 the input frequency when the loop is locked. A crystal-controlled oscillator is used so that it will not drift outside the loop lock-in range under unlocked conditions nor produce a large loop error when the loop is locked.

The oscillator circuit uses a common base amplifier parallel resonant in the collector circuit. A portion of the output current is fed back to the emitter through a series tuned circuit to sustain oscillations. Frequency stability and control is determined in the feedback circuit which is extremely narrow band whereas the collector anti-resonant circuit is relatively low Q. The feedback circuit consists of a crystal series resonant at exactly the oscillator center frequency, two series varicaps (voltage controlled capacitors) and an inductor. The inductor and varicaps are also series resonant at approximately the center frequency. Any change in varicap capacity, caused by a voltage change from

the loop filter, pulls the center frequency of the feedback circuit thus changing oscillator frequency.

The two multipliers, X6 and X4, use conventional common emitter amplifiers. Each is biased for maximum multiplication efficiency at the available driving power level. The collector circuits are parallel tuned at the respective output frequency. The first multiplier uses a double-tuned output circuit for greater harmonic efficiency.

The X58 multiplier loop is shown in SCI Drawing 362141. The VCO, phase detector, and X2 circuits are similar to those just discussed in the Divide-By-24-Loop except that a third overtone crystal is used in the 33.959 VCXO.

The PCO (pulse controlled oscillator) multiplier consists of the LC oscillator Q9 and switching transistor Q8. In addition, a PCO driver is made up from buffer amplifier Q5 and Schmitt trigger Q6 and Q7. Diode CR6 clamps the switching transistor base to the positive supply voltage and prevents reverse voltage from breaking down the base-emitter junction of Q8. Isolation amplifier Q10 prevents excessive loading of the PCO and provides the necessary signal level to the phase detector input. Capacitor C41 is the PCO frequency tuning ad-

justment. The center frequency of the LC tuned circuit containing L3 and C41 determines the exact frequency component which is emphasized most in the PCO output spectrum.

The X76 Multiplier Loop is shown in SCI Drawing 362162. This loop is similar to the X58 loop except for use of a simple DC amplifier following the phase detector and the use of high-frequency high-performance FD-700 switching diodes in the phase detector. In addition, a X2 multiplier is included in the phase lock loop feedback circuit to allow movement of the output frequency in increments of 1/4 f_o as discussed in the Theory of Operation section. Design of the X76 Loop is perhaps the most difficult of all the multipliers in the Transponder due to the high PCO frequency, high PCO multiplying factor, high phase detector frequency, and high VCXO operating frequency.

5.1.6 X32 Multiplier

The X32 multiplier was purchased from Microwave Associates. Specifications for the multiplier are listed below:

Input Frequency	67.918 mc
Output Frequency	2173.376 mc

Input Power	10 mw
Output Power	10 mw
DC Supply Voltage	+20 V
Spurious Suppression	More than 30 db
Temperature	-20 to +70°C
Size	1.6 x 3.0 x 9.0 inches
Output Connector	Type N
Input Connector	Type TNC
Power Connector	Bendix

5.1.7 Range Tone Circuits

The 2.342 mc and 2.2688125 mc Range Tone Loops are shown in SCI schematic drawings 362007 and 362016. These loops are essentially similar except for the limiter in the signal input amplifier, Q11, in the 2.2688125 mc loop. The phase detectors, VCO's, DC amplifiers, and other circuits are the same except for operating frequency and/or slightly different adjustment of phase detector gains as discussed in Section 4.2. Loop bandwidths are the same at threshold but the 2.2688125 mc limited loop becomes somewhat wider at higher input S/N ratios.

The output of the 2.342 mc phase detector contains the demodulated coarse range tone signals at 1.1078 kc and

1.1793 kc. Therefore, this output is fed to the active filter on the Sideband and Identification Generator board (SCI Drawing 362116).

The DC operational amplifier consists of eight transistors and three zener diodes. The 2N2453 input transistor is actually two matched transistors in a single TO-5 case. The amplifier is a differential balanced type with input and output voltages nominally centered at zero. This type circuit requires both +20 and -20 volts DC for proper operation. Temperature stability is obtained by use of the matched input transistors and by use of a large amount of negative feedback. A current source formed by Q9 and the associated circuitry insures a high degree of coupling between the two differential amplifier sections and thus improves stability and common-mode signal rejection.

The active filter for the 1.1078 and the 1.1793 kc signals is shown in the lower left corner of SCI Drawing 362116. The requirement for this filter was to produce a very sharp cut-off circuit either side of two pass frequencies at 1.1078 kc and 1.1793 kc. The circuit operates over the range of -20 to +70°C and over this range has an output stability of ±10% in amplitude and ±1° in phase shift. An attenuation of 20 db is required be-

tween the pass frequencies and the narrowest possible band outside the pass frequencies. The input impedance is not less than 100k ohms.

The factor which most affects design is the phase shift stability requirement. Considering the 6 db bandwidth of a tuned filter, the phase shift which occurs between 6 db points is 120 degrees. This is to a first order of accuracy a linear phase change with frequency. The bandwidth to obtain the required attenuation between pass frequencies has to be in the order of 30 cycles in a practical circuit. Thus, the rate of change of phase shift with frequency is 4 degrees per cycle, giving a frequency stability requirement for the filter of not greater than ±0.25 cycles or ±.022 percent.

The circuit which has been chosen to produce the necessary characteristics uses two LC tuned circuits in a Q multiplying feedback circuit. The filter amplifier consists of two transistors Q7 and Q6 in a feedback pair, giving high input impedance and a stable gain of approximately three. The output is fed back to the input in positive phase to multiply the Q of the two tuned circuits formed by L4 and L5 and their associated capacitors. The values in the circuit are dictated by the input

impedance requirement and the maximum tuned circuit impedances obtainable. The tuned circuits have to be DC blocked to maintain the DC bias conditions of the amplifier and the feedback path is DC blocked to prevent low frequency instability due to series resonance of the tuned circuits.

The value of the feedback resistor R22 gives control of the Q and hence the bandwidth of the overall circuit. It has a critical value in the region of 15K ohms where the greatest Q is obtained. To obtain a 30 cycle bandwidth, the circuit is detuned by using a 47K ohm resistor.

An output stage Q8 is provided to raise the output signal to the required voltage and power levels.

To meet the stability requirements special care was necessary in the selection of components for the tuned circuits. An inductor wound on a stabilized toroidal core is used. This core material gives a controlled linear positive coefficient of inductance with temperature. The inductance is tuned with a composite capacitor composed of polystyrene and mica capacitors. The temperature coefficient of polystyrene capacitors is almost equal and opposite to the temperature coefficient of the inductor while the mica capacitors have a small positive coefficient. There-

fore, the change in inductance is nearly compensated by the change in the polystyrene components and exact compensation is achieved by empirically adjusting the polystyrene to mica ratio in the composite capacitor. The two tuned circuits are adjusted individually and there is little interaction between the two when connected in series. The slight shift of center frequency which occurs is readily padded out without interfering with the temperature compensation. For practical purposes, the center frequencies are set at the zero phase shift points since the zero phase shift and peak amplitude points are not coincident in the compound tuned circuit. Since similar inductors are used for both frequencies, a series resistor is added in the higher frequency circuit to equalize the amplitude of the two peaks.

The 2.2688125 mc identification generator crystal oscillator also appears on Drawing 362116. This oscillator uses a series-mode crystal in a two-transistor emitter-coupled circuit. Output of the oscillator is gated by the shunt modulator consisting of transistors Q3 and Q4. The input to Q3 is from the site identification code generator in the Command Logic equipment. The crystal oscillator is also gated on or off for different operating modes by the Range Tone Gate input to gating transistor Q14 and the diode CR1. Output of the 1.1078 and 1.1793 kc filter is also

gated on or off by the same input.

The 2.342 mc signal from the Range Tone Loop is remodulated with the 1.1078 and 1.1793 kc signals from the active filter in the modulator/combiner circuit consisting of Q10, Q11, Q12 and the resistive adder network R43 and R45. The AM modulator produces the required output spectrum but with too much 2.342 mc carrier amplitude to meet the output spectrum amplitude requirements. Therefore, a 180 degree phase shift is added to the 2.342 mc carrier and the phase shifted carrier is combined with the AM modulator output to reduce the output carrier amplitude to the specified level. The modulator is similar to a beam-switching tube-type modulator in that transistors Q10 and Q11 turn the current on and off in coil L6 while the modulated current source Q12 controls the amount of current through L6 in accordance with the modulating signal from the active filter.

5.2 Transmitter

5.2.1 Transmitter Tracking Filter

This module contains the 28.104 mc Tracking Loop, the Doppler Reverser, and a Divide-By-24 Loop (see Transmitter Block Diagram). The Divide-By-24 Loop has been discussed in

Section 5.1.5. The Tracking Loop and the Doppler Reverser will be discussed in this section.

All the 28.104 mc tracking loop circuitry except the VCO is shown in the Tracking Loop Schematic (362039). The phase detector, driver amplifiers, and loop filter are similar to circuits which have already been covered in previous sections. The loop filter is a passive type consisting of R9, R13, R14, and C14. Additional circuitry included to provide a visual indication of loop lock consists of a coherent amplitude detector followed by a Schmitt trigger. No output is obtained from the amplitude detector unless the tracking loop is locked. The Schmitt trigger output is approximately +18 volts when the loop is not locked, and is very small (less than 1 volt) when the loop is locked.

The Doppler Reverser circuits (362064) were designed with particular attention to minimizing spurious signal feedthrough to the outputs. The X4 multiplier is made up from two doubler stages each of which uses two transistors with push-pull input and paralleled outputs. Thus the fundamental and all odd-order harmonics are balanced out and do not appear in the outputs with any significant amplitude. The two mixers are balanced to both input signals so that these signals do not appear at the mixer out-

puts. The summing mixer consists of transistors Q8 and Q9. The $8 f_o$ and $12 f_o$ signals are fed to buffer amplifiers Q6 and Q7, respectively and are linearly added in the primary of transformer T3. Thus both signals are fed to the balanced input of the mixer and are cancelled out at the mixer output. This mixer output is tuned to $20 f_o$ by L6 and C34. Impedance matching to the next amplifier Q10 is accomplished by selecting the ratio of C33 and C34. The output of Q10 at $20 f_o$ feeds the subtracting balanced mixer composed of transformer T_4 and diodes CR5 and CR6. The other input to this mixer at $32 f_o$ is fed to the center tap of transformer T4 so that it is also balanced out at the mixer output. The mixer output then feeds common-base amplifier Q11 and buffer amplifiers Q12 and Q13. The Doppler Reverser output is switched off by removing the +5 volt control signal from the Doppler Compensation Gate input. The application of the +5 volt control signal reverse biases diodes CR3 and CR7 so that normal operating base biase is applied to transistors Q7 and Q11. The removal of the +5 volt control signal by shorting the Doppler Compensation input line to ground through a low impedance results in the reduction of base bias to Q7 and Q11 to a point where the transistors are non-operative and will not pass a signal.

5.2.2 Tracking VCO and Reference Oscillator

The 28.104 mc VCXO has been described in Section 5.1.4. The VCXO in this module is identical to the one used in the receiver. The VCXO distribution amplifier contains three conventional common-emitter amplifiers to provide the required power output and isolation of the VCXO from the loads. See SCI Drawing 362028 for schematic diagram. Output No. 1 feeds back to the 28.104 mc phase detector in the transmitter tracking loop; output No. 2 feeds the Divide-by-24 Loop in the Transmitter Tracking Filter module.

The 18.736 mc (8 f_o) Reference Oscillator and its buffer amplifier are also contained in this module. Schematic diagram number 362048 shows the oscillator circuit. The buffer amplifier appears in schematic number 362072.

The 18.736 mc oscillator is an unusual circuit which has some distinct advantages in frequency and amplitude stability. The circuit is a series resonant crystal oscillator built around an emitter-coupled differential amplifier. Emitter coupling gives symmetrical limiting and a relatively constant high output impedance.

The factor which adversely affects frequency stability

in an oscillator is phase shift in elements other than the controlling element. If all phase shifts other than controlling elements are considered as a tuned circuit of a given Q, called Q_S, and the crystal is considered as a tuned circuit of a higher Q, called Q_X, then the oscillator drift due to causes other than the crystal is given by the equation:

$$\Delta f_{oscillator} = \Delta f_{circuit} \left(\frac{Q_S}{Q_X} \right)$$

Since Q and phase shift are proportional, unnecessary phase shift should be kept to a minimum.

The limiting action of the differential amplifier is such that the output is a square wave of current from a high impedance source. Since there is little second harmonic in the output current, a low-Q filter can give a clean output signal. Since this filter is in the frequency controlling loop making it low Q improves stability. There is little phase error introduced by the limiting action. This again insures good stability.

Referring to the schematic, SCI-362048, it can be seen that Q1 and Q2 form a differential amplifier which is emitter coupled by R8. R6 is used to give a proper load to the crystal and R7 is used to balance the no-signal currents and to insure starting.

The output of Q2 is taken out through T1. C5 is used to resonate the primary of T1, forming the low-Q filter needed to insure a clean output. The output of T1 is fed to the base of Q1 through a series-resonant crystal and a series-resonant trimming network formed by L1, C2 and C11. Zener bias is used to stabilize the frequency against incidental FM produced by power supply noise and drift.

The buffer amplifier is a common-base amplifier padded to provide unity power gain. The common base stage gives the best isolation of the three one-transistor configurations if the transistor is used well below Alpha cutoff. Zener bias is used on the buffer to further reduce the effect of power supply noise on the reference oscillator.

5.2.3 Transmitter Synthesizer

The Transmitter Synthesizer consists of two PCO multiplier loops similar to those previously described in the Receiver Synthesizer module. The X60 Loop is shown schematically in SCI Drawing No. 362091, and the X57 Loop is shown in Drawing 362139.

Output from the X60 Loop can be changed in increments of $1/4\, f_o$ as explained in the Theory of Operation. Output

from the X57 Loop can be changed in increments of 1/2 f_o.

Bandwidths, tracking range, maximum static phase error, and other loop parameters are tabulated in Section 4.2.

5.2.4 Spectrum Generator No. 1

The X4.8 and X6.0 Loops are contained in this module. The X4.8 is shown schematically in SCI Drawing 362146 and the X6.0 in Drawing 362148. These two multiplier loops are essentially identical except for the slightly different operating frequencies. Both loops have a X5 multiplier in the feedback path of the phase lock tracking loop and therefore provide capability of changing the output frequencies in increments of 0.1 f_o. The method of changing output frequencies is described in detail in the Theory of Operation in Section III of this report.

These multiplier loops contain provision for external switching of the output from the Channel Selection information from the Transponder Site Command Logic. A solid-state switch utilizing a diode to turn off the VCO when no command signal is present, and to turn on the VCO when the +5 volt channel selection signal appears is incorporated in all the multiplier loops in the spectrum generator modules. In order to assure that the VCO is turned off, a low-impe-

dance (50 ohms or less) path to ground is required at the channel selector switch input terminal. This condition will normally be met when the Command Logic and the Transponder are interconnected for system operation. However, for individual tests of the Transponder it will be necessary to provide temporary shorting plugs on the channels not being used. Then when the +5 volts is applied to the operating channel, the operation of only that channel is assured.

5.2.5 Spectrum Generator No. 2

The X10.6 and X11.8 Loops are contained in this module. The X10.6 is shown in SCI Drawing 362151 and the X11.8 in Drawing 362153. Circuits and design of these loops are essentially identical to the X4.8 and X6.0 Loops described in the previous section except for slightly higher operating frequencies.

5.2.6 X32 Multiplier

The X32 Multiplier was purchased from Microwave Associates. Specifications for this unit are given below:

Input Frequency	66.747 mc
Output Frequency	2135.904 mc

Input Power	10 mw
Output Power	100 mw
DC Supply Voltage	+20 V
Spurious Suppression	more than 30 db
Temperature	-20 to +70°C
Size	1.6 x 3.0 x 9.0 inches
Output Connector	Type N
Input Connector	Type TNC
Power Connector	Bendix

5.2.7 Transmitter Modulator

5.2.7.1 Transmitter Mixer

The AROD Transmitter Mixer consists of the following basic sections (refer to SCI Drawing No. 362042 and 362097):

(1) 5.62 mc to 13.82 mc Wideband Amplifier

(2) Balanced Modulator

(3) 70.26 mc Narrow-Band Amplifier

(4) 75.88 mc to 84.08 mc Band-Pass Filter

(5) 75.88 mc to 84.08 mc Wideband Amplifier

The 5.62 mc to 13.82 mc Wideband Amplifier stage consists of two transistors in common-emitter configuration.

Current feedback is utilized to achieve a suitable bandwidth and power output. The current feedback is achieved by connecting a resistor and a by-pass capacitor from the emitter of the output transistor to the base of the input transistor. The feedback resistance is varied for an optimum and flat output from 5.62 mc to 13.82 mc. A sweep generator was used to observe the output.

The design of this type of amplifier is straightforward and adjustments are not extremely critical. The amplifier is quite stable and easily reproduced. There was no detectable difference in performance between the breadboard and final design circuits.

The Balanced Modulator consists of two 2N918 transistors with their collectors tied together and the output taken from a low Q transformer connected to the collectors. The low-frequency signal (5.62 mc to 13.82 mc) is impressed on the base of one transistor (Q3) and the emitter of the other (Q2). The high frequency (or carrier) signal of 70.26 mc is impressed on the base of transistor Q2 and the emitter of transistor (Q3). Since there is no phase inversion in a common base circuit and 180^{o} phase difference in a common emitter circuit, a signal impressed on the base of one transistor and the emitter of the other

will produce two signals 180° out of phase. Since the collectors are tied together, the signals will cancel out if they are of equal magnitude.

To achieve equal magnitude of the two signals, capacitors are placed from the emitter of one transistor to the base of the other. Adjustment of these capacitors will vary the magnitude of the two 180° out-of-phase signals.

Optimum performance of this balanced modulator is achieved through the adjustment of the above mentioned capacitors and the selection of signal levels from the modulating and carrier inputs. The adjustments of this modulator are not critical. However, the Q of the output transformer must be fairly low in order that the desired upper-sidebands of 75.88 mc to 84.08 mc be of the same output level.

The carrier rejection of this circuit was found to be at least 15 db. This is sufficient rejection since the bandpass filter used has a carrier rejection of an additional 25 db. Thus, the total rejection meets the design goal of 40 db.

This type of balanced modulator circuit was not the only type considered. A diode bridge type of balanced modulator

was also considered. However, the diode required for the high frequencies involved costs more than a 2N918 transistor. Since four such diodes are utilized in a bridge modulator, the cost would be more than twice that of the circuit used. There was also no appreciable advantage in using a diode bridge since all specifications can readily be met with the circuit used. Another advantage of the two-transistor type of modulator used is that it has power gain whereas the diode modulator has conversion loss.

The 70.26 mc narrow-band amplifier is used for the dual purpose of isolation and to provide the suitable input level to the balanced modulator.

The circuit is a single stage, common emitter amplifier. The amplifier used supplies approximately 7 db gain into a 50 ohm load.

The output of the balanced modulator consists of upper and lower sidebands and a suppressed carrier. A band pass filter is used to eliminate the lower sideband and carrier and to pass the upper sidebands of 75.88 mc to 84.08 mc.

The band pass filter attenuates the carrier by 25 db and the lower sidebands by 50 db. The output is flat from 75.88

mc to 84.08 mc with an insertion loss of less than 1.5 db. Ultimate attenuation of frequencies outside the passband is greater than 40 db.

It is essential that a filter at this range of frequencies be placed within a shielded container. The size of the container is dictated by the size and number of elements used in the filter.

An M derived filter was designed to theoretically meet the required specifications. However, as is generally the case in constant K or M-derived filters, the experimental results did not agree with calculated performance. The filter rejected the lower sidebands by 40 db but only rejected the carrier by 13 db instead of the required 25 db. The attenuation through the pass band was 4 db. The impedance of the filter, which was designed for 50 ohms, varied through the rather wide pass band.

A (n = 6) Butterworth filter was then designed and evaluated. This filter performed better than the M-derived filter in that its impedance remained very close to 50 + j 0 through the pass band. It also presented higher attenuation to the lower sidebands. However, as in the case of the M-derived filter, the skirts were not steep enough to reject the carrier by 25 db.

Because of the limited time available for optimization, it was decided to purchase the required filter from Aladdin Industries. The cost of their filter is less than that of the SCI filter and the size is smaller. The Aladdin filter is 1/2" x 1/2" x 3", whereas the SCI filter is 1/2" x 1" x 3 1/2". Even more important, the Aladdin filter rejects the carrier by more than 25 db.

The design specifications of the Aladdin filter are as follows.

The insertion loss over the pass band of 75.88 mc to 84.08 mc shall not exceed 1.5 db maximum.

The insertion loss at 70.26 mc (the carrier frequency) shall exceed 25 db minimum.

The insertion loss from 55 mc to 65 mc (the lower sidebands) shall exceed 50 db minimum.

The insertion loss below 55 mc and above 100 mc shall exceed 40 db minimum.

The input and output impedance of the filter shall be 50 ohms nominal.

The Aladdin filters were checked by SCI and were

found to meet or exceed these specifications.

Other methods of removing the lower sidebands were considered. However, these methods such as phasing methods, are much more elaborate and less reliable. The filter method is simple, economical and since the filter is composed of only passive elements, it is inherently more reliable. The filter is also physically small and requires no tuning or adjustments whatsoever. A phasing type of sideband rejection would require tuning and is difficult to adjust at these frequencies.

Since there is an excess of power available, the slight loss through the filters (approximately 2 db) is not in any way critical.

The 75.88 mc to 84.08 mc wide-band amplifier is used as an output buffer stage and also provides the required signal level to the next section. This stage is of the same configuration and has the same operating description as the 5.62 mc to 13.82 mc wide-band amplifier previously described. The basic difference is that higher frequency (2N918) transistors are used.

Only one stage (two transistors) is required to provide the signal level required in the next section.

Other types of wide-band amplifiers were tried and rejected for various reasons. One type of amplifier tried used a staggered-tuned amplifier. This was rejected for the following reasons:

(1) The output power and bandwidth required can be achieved by the more simple current feedback stage.

(2) The stagger-tuned amplifier was found to be extremely critical with respect to undesired regeneration.

(3) The tuning and adjustments of the stagger-tuned amplifier are tedious, time consuming and very critical.

(4) The L and C elements used in the tank circuits are critical and the physical placement of these elements are extremely critical.

(5) Such an amplifier was found to be extremely hard to reproduce.

Shunt, series, and combinations of compensated amplifiers were considered and rejected because of their tendency to

oscillate and the criticality of their elements and physical placement.

Resistance Tee attenuators were used for matching purposes throughout the transmitter-mixer. This was done since a properly designed resistance Tee presents a constant impedance for all frequencies. This is quite important since it minimizes feedback and the possibility of oscillation.

The power into this system was approximately 6 dbm for each modulating frequency and carrier. The required power output was -3 dbm. Since there is then an excess of power in the system, the Tee pads perform the dual function of matching and of attenuation. They also eliminate the need for more critical reactive elements.

Several 2N918 transistors in common emitter configuration were used in this system. The V_{ceo} of the 2N918 is 15 volts while the supply voltage is at 20 volts. Care was taken in the bias design of these stages in order that V_{ceo} did not exceed the specified maximum.

The reason for using these transistors in common emitter configuration is because of the requirement for negative

current feedback. The common emitter configuration provides a simple method of obtaining the desired negative current feedback.

The filters purchased from Aladdin, while exceeding the performance of the filters designed by SCI, still do not have an exactly flat loss across the pass band. To compensate for this, a variable piston capacitor was placed in the transformer circuit of the balanced modulator. This capacitor is then adjusted for maximally flat output. Even so the output of the transmitter-mixer has a slight droop (of about 0.7 db) across the output of 75.88 mc to 84.08 mc. However, this has been compensated for in the next section (the Single Sideband Generator and Linear Power Amplifier).

The design goals in this system were to produce an output signal of -3 dbm while suppressing all spurious signals by 40 db. This was achieved for all modulating frequencies except the lowest (i.e., 5.62 mc). With a modulating frequency of 5.62 mc, the spurious signal is down only -35 db.

The placement of monitor points presented a slight initial problem. It was the original intention to place a monitor point after each input amplifier (i.e., on the output of the 70.26 mc amplifier and the output of the 5.62 mc to 13.82 mc amplifier).

One of the four carrier frequencies at 32.4 f_o, 33.0 f_o, 35.3 f_o, or 35.9 f_o is fed into the other inputs of the above balanced modulators. The input to one balanced modulator is direct and to the other balanced modulator is through a 90 degree phase shift network which consists of a coaxial delay line (DL1). In order to provide fine trimming of the 90 degree phase shift for each of the four carrier signals, a small adjustable phase trimmer is provided for each carrier frequency. These phase trimmers consist of varicaps CR17 and CR18, and the gated voltage dividers which are actuated by the Channel Selection Logic inputs.

The balanced modulators use the Hewlett-Packard HP-2103 "Hot Carrier" diodes to provide fast switching action and good modulation efficiency in the operating frequency range from approximately 75 to 85 mc. The output of this type balanced modulator is relatively independent of carrier level after a sufficiently high input level is reached. Therefore, slight differences in level on the four different channel carriers does not appreciably affect the output sideband level from the single sideband generator.

5.2.7.3 Linear Power Amplifier

The 75-85 mc Linear Power Amplifier schematic is shown in SCI Drawing 362113. This amplifier is broadband and

The desired DC monitor point voltage is 0.5 to 1.0 volts. This could not be met at the originally intended points. The monitor points were then moved to the inputs of the board and met the requirements.

5.2.7.2 Single Sideband Generator

The phasing-type sideband generator is shown schematically in SCI Drawing 362094. The two balanced modulators and associated circuitry are arranged to balance out the carrier and upper sideband components. Output from the sideband generator thus consists solely of lower sideband components. The carrier component is reinserted at a later stage of the transmitter to produce the required output spectrum of carrier plus lower sidebands.

The modulated 2.342 mc signal and the 2.2688125 mc signal are combined in a linear adder and the combined signals are applied to one of the balanced modulators. The modulated 2.342 mc signal and the 2.2688125 mc signal are also shifted in phase by 90 degrees and combined in another linear adder before being applied to the other balanced modulator. Trimmer capacitors C2 and C4 allow individual adjustment of the phase shifters to provide exactly 90 degrees phase shift.

entirely class A to provide the necessary linearity with peak power outputs greater than 250 mw. The broad bandwidth is obtained by use of a flat staggered triple and the high power output is obtained from a pair of 2N2222 transistors operating in common-base push-pull configuration. Maximum possible gain-bandwidth product is achieved by resonating the collector tuned circuit with only the transistor output and stray circuit capacity. This technique coupled with the inherent gain in L/C ratio due to the push-pull connection allows an excellent gain-bandwidth product to be obtained in the output stage. Thermal heat sinks are used to hold down the transistor junction temperature.

A linear adder at the power amplifier input combines the lower sidebands from the Single Sideband Generator and the carrier component from the Transmitter Mixer to produce the required output frequency spectrum. The linear adder consists of two common-base stages feeding a common collector tank circuit. The signals are thus linearly combined by a circuit arrangement which assures maximum isolation of the signal sources from each other.

The output of the Linear Power Amplifier is somewhat greater than 50 mw average with the required complex signal spectrum which has a peak-to-average power ratio of about 7 db.

5.2.8 S-Band Mixer

The S-Band Mixer was purchased from Sanders Associates. The unit employs stripline techniques for both the balanced mixer and the associated filter which are built into a single package. Specifications for the mixer are given below:

> S-Band Mixer and Filter, in accordance with Sanders Associates Quote No. 73EE except the following:
>
> 1. 76 to 84 mc input to employ type TNC connector.
> 2. Four mounting holes to be provided, one in each corner.
> 3. Linearity to be 5% or better for output power or 10 mw. Design goal to be 1%.

In order to more fully explain the specifications, a copy of Sanders Quote No. 73EE follows:

TECHNICAL DISCUSSION FOR A SINGLE SIDE BAND MODULATOR

To meet the requirements of the Single Side Band Modulator, which are delineated in the attached Specifications, a Balanced Modulator followed by a Bandpass Filter is proposed. This is shown in Figure (1). A fixed frequency at approximately 2135.8MC will be fed into Connector (A) of the assembly. Up to five (5) modulating signals in the 76 to 84MC region will be fed into Connector (B). The desired upper side band in the 2209 to 2219MC will emerge from Connector (C).

An upper side band power level of 10mw can be obtained for a single modulating signal of about 100mw with a carrier level of about 100 mw. This corresponds to a 10db overall conversion level. The Modulator itself should have about 9db loss with 1db loss in the Bandpass Filter. However, to achieve 10mw output for each of two or more simultaneous modulating signals may require slightly more modulating and carrier signal power. For all five (5) modulating signals applied simultaneously, it is estimated that approximately 125mw may be required for each of the modulating signals as well as the fixed frequency carrier signal. This will have to be determined empiracally after the Modulator is designed. An attempt will be made to design the Modulator for minimum conversion loss with multiple modulating signals. However, due to the unusual nature of this device, an overall 10db conversion loss cannot be guaranteed.

In order to handle the anticipated input power, cartridge type diodes must be employed. However, if overall package size and weight are important, it may be worth considering the use of internally mounted glass envelope diodes, such as 1N831. These diodes would

limit the total input power, carrier plus all modulating signals, to about 700mw. With no more than four (4) simultaneous modulating signals, there should be no problem in achieving the required 10mw output for each side band. However, with all modulating signals applied, the drive power may have to be reduced below that which will provide 10mw output for each side band. It is estimated that at least 8mw can be provided under these conditions. The saving in size is primarily that required for the cartridge diodes, shown in Figure ( ). The weight reduction possible with internally mounted diodes is approximately 2 ounces. In either case, the diodes will be field replaceable in case of accidental damage.

Response for a typical Balanced Modulator is shown in Figure (2). This data was taken on an experimental L-band unit with a modulating frequency in the 54MC region. Over a 30% bandwidth, the conversion loss variation was in the order of 1/2db. Similar performance should be expected from the proposed Side Band Modulator for any one modulating signal.

TRI-PLATE® Strip Transmission Line Techniques will be used for both the Balanced Modulator and the Bandpass Filter. This will provide a very rugged, easily reproducable assembly that is consider ably smaller and lighter than other transmission line techniques can provide. There is a great latitude in package configuration. The tentative outline drawing enclosed shows the approximate volume required if a two (2) layer assembly is employed. That is, the Modulator Circuit and Bandpass Filter are coplanar with internal feed through connections. An alternate configuration could be provided in which both circuits are in a single layer. This would require approxi-

2. Power:

a) Input @ Connector (A):	100mw, minimum
b) Input @ Connector (B):	Approximately 125mw for each frequency component.
c) Maximum Input Power in Connectors (A) & (B):	900mw
d) Output @ Connector (C):	10mw minimum for each frequency component.

3. Unwanted Output Signal Suppression:

Both the RF Carrier (input A) and the lower side band frequencies in the vicinity of 2055MC will be suppressed by at least 45db below the desired output frequencies power level.

4. Modulation Linearity

a) For equal amplitude signals (f_o & $f_o - f_m$) in Connector (B) within the frequency range listed in paragraph 1.b. above, the output upper side bands at Connector (C) will be equal within 0.5db.

b) A signal power variation between 50 and 130mw for each frequency at input Connector (B), the conversion loss will not vary more than ±1db.

5. Temperature: $-20^{\circ}C$ to $+70^{\circ}C$

6. Size: Approximately 4-1/2" X 3-3/4" X 9/16", excluding connectors.

7. Weight: Approximately 1 pound.

8. Connectors: Type N female, mounted as shown in Figure (1), but not necessarily in the exact position shown.

mately twice the area with about 1/2 the thickness. Location of the two (2) input and the output connectors can be varied to some extent. Mounting holes can also be provided at the four (4) corners.

TRI-PLATE Techniques employed by Sanders Associates, Inc. permit the use of various dielectric materials. For this application, a linear (irradiated) polyolefin material is proposed because of its low loss and uniform dielectric properties. Over the upper side band frequency range (2209.4 to 2219.8MC) the filter will be designed to have essentially flat response characteristics, increasing no more than 0.1db at the passband edges. Passband ripple should not exceed a few tenths of a db. The actual insertion loss of the filter over the passband is expected to be approximately 1db.

SPECIFICATIONS

SINGLE SIDE BAND MODULATOR

1. Frequencies:

   a) Input @ Connector (A): 2135.804MC

   b) Input @ Connector (B): f_o and $f_o - f_m$

      where $f_o = 80 \pm 4$MC

      and f_m = 2.2688, 2.342MC & two (2) other frequencies in between.

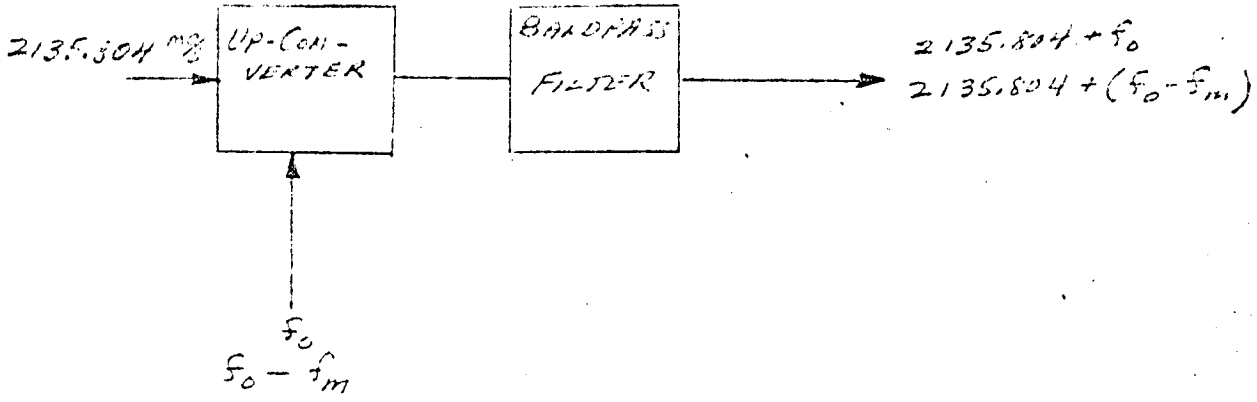
   c) Output @ Connector (C): $2135.804 + f_o$ & $2135.804 + (f_o - f_m)$

SPECIFICATIONS

SANDERS ASSOCIATES

DATE 9-6-63

Quotation No. 73EE

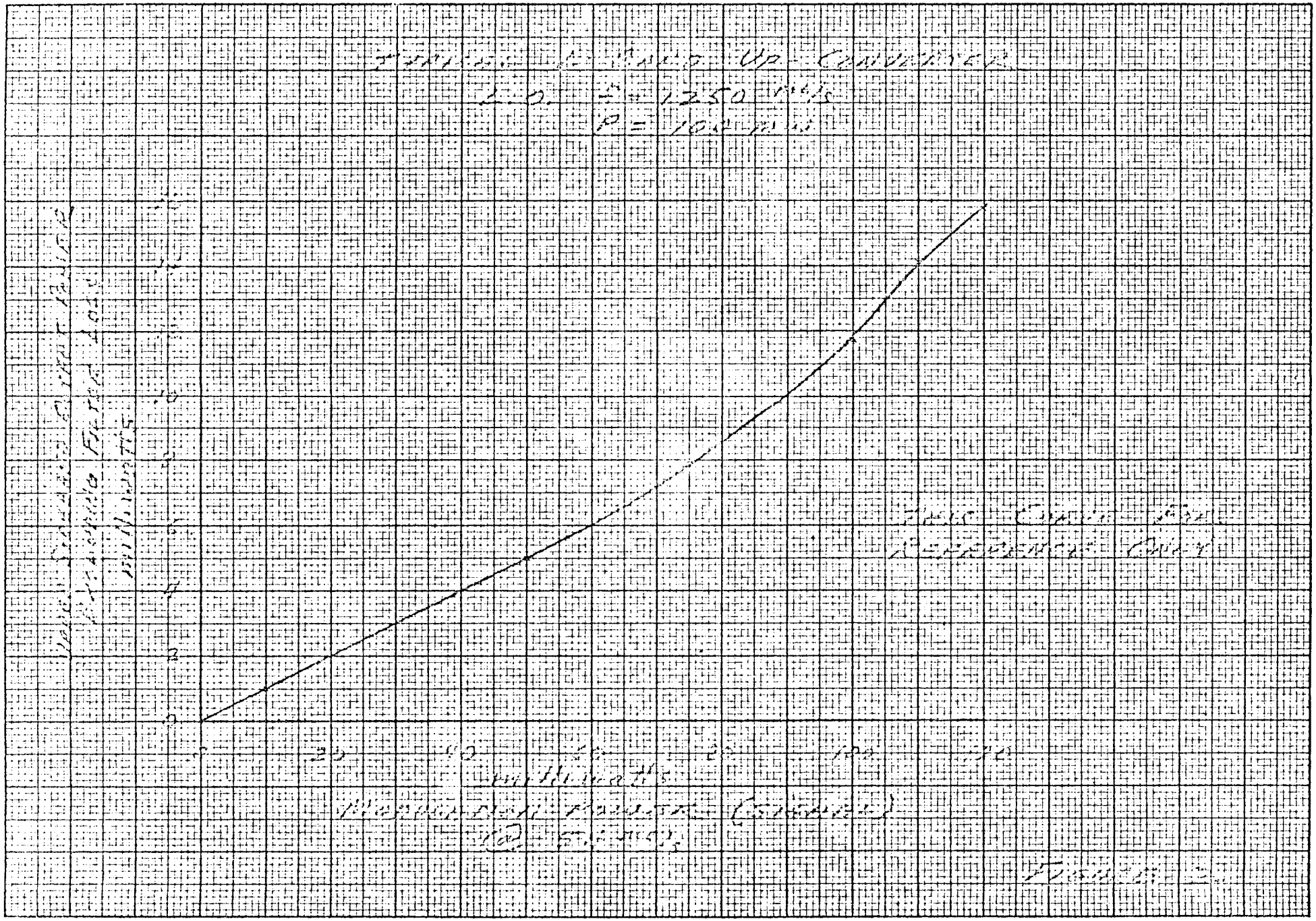


f_o = 76 TO 84 mc/s

f_m = 2.342 AND 2.2[illegible] mc/s
PLUS TWO IN BETWEEN

BLOCK DIAGRAM
QUOTE # 73EE
FIGURE 1

SANDERS ASSOCIATES, INC.
MICROWAVE PRODUCTS DEPARTMENT, 95 Canal Street, NASHUA, NEW HAMPSHIRE, Telephone: Tuxedo 3-3321



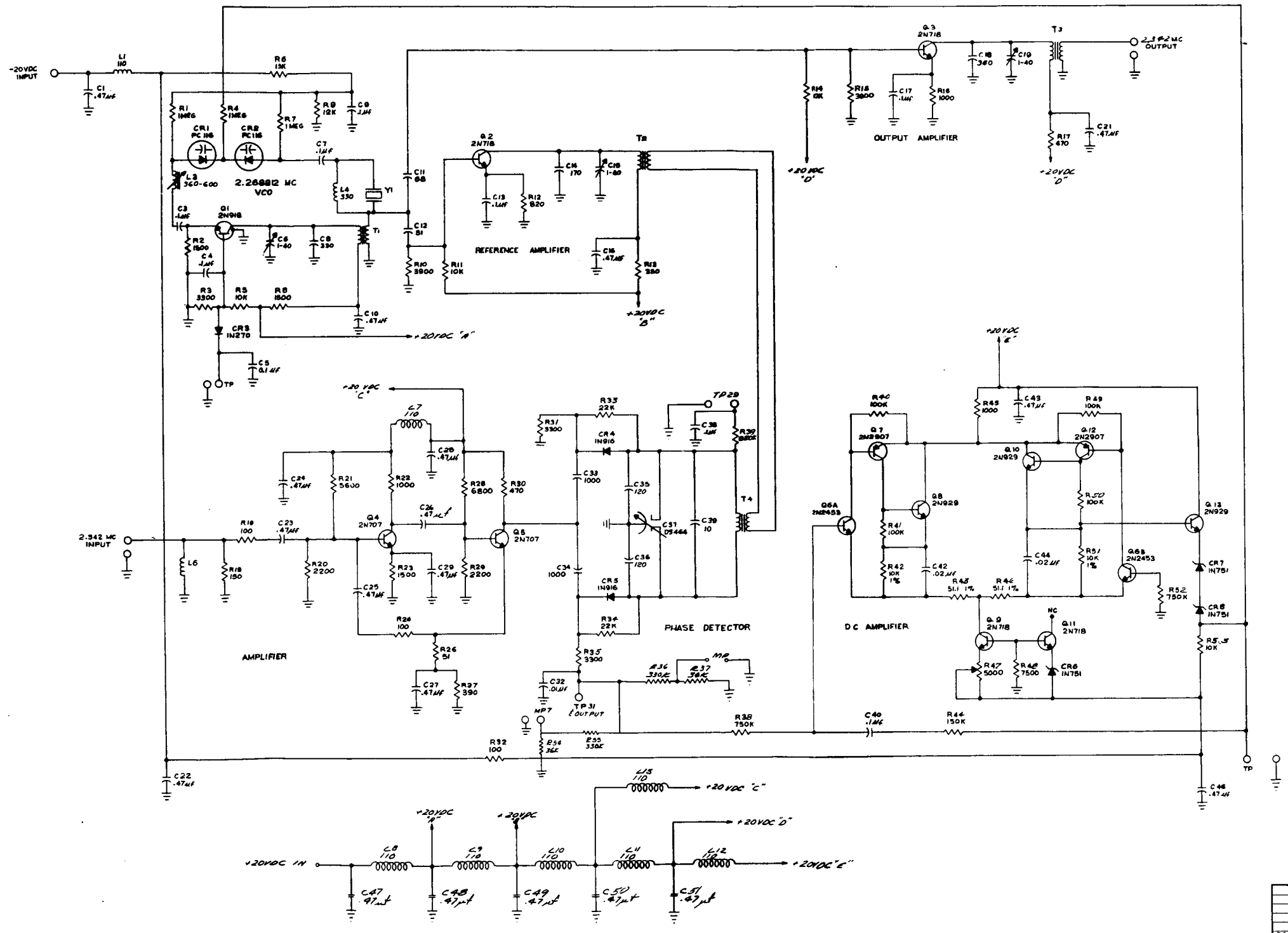
LIST OF DRAWINGS

Block Diagrams	SCI Drawing No.
Receiver Block Diagram	362034
Transmitter Exciter Block Diagram	362042

Schematics	SCI Drawing No.
2.342 MC Range Tone Loop	362007
Divide by 24 Loop	362009
2.2688124 MC Range Tone Loop	352016
Tracking Loop VCO Distribution Amplifier	362028
Receiver Distribution Amplifier	362031
Tracking Loop	362039
Reference Oscillator	362048
Doppler Reverser	362064
First IF Amplifier	362069
Reference Oscillator Buffer Amplifier	362072
Sideband Demodulator	362075
Main Loop Filter	362082
Carrier Demodulator	362085
Second IF Amplifier	362088
X60 Multiplier Loop	362091
Single-Sideband Generator	362094

Schematics	SCI Drawing No.
Transmitter Mixer	362097
Sideband IF Amplifier	362100
Carrier IF Amplifier	362105
AGC Demodulator	362108
Linear Power Amplifier	362113
Sideband and Identification Generator	362116
X57 Multiplier Loop	362139
X58 Multiplier Loop	362141
X4.8 Multiplier Loop	362146
X6 Multiplier Loop	362148
X10.6 Multiplier Loop	362151
X11.8 Multiplier Loop	362153
X76 Multiplier Loop	362162
28.104 mc VCXO	362180

SYM	DESCRIPTION	DATE	APPROVAL
A	REVISED	2-14-64	



NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μF
3. ALL INDUCTORS ARE IN μH
4. LAST REFERENCE DESIGNATIONS USED:
R55; C51; CR8; Q13; T4; Y1; L13
5. REFERENCE DESIGNATIONS NOT USED
C2, C20, C30, C31, C41, C45, L2, L5, R25

A-02241

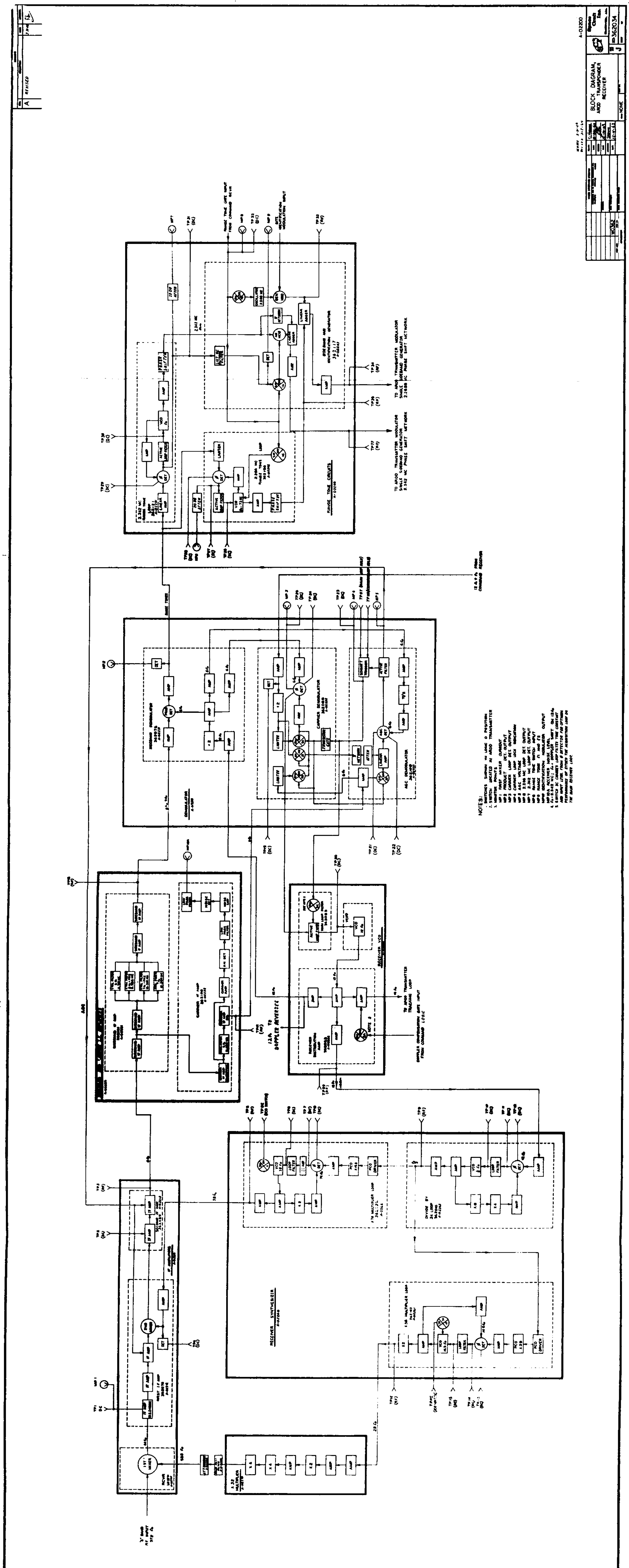
362008	W0362	C. Hodges	27-JAN-64
			2-10-64
			2-10-64
			3-6-64

SCHEMATIC
2.342 M C RANGE TONE LOOP

Space Craft Inc.
Huntsville, Ala.

SIZE	DRAWING NO.	REV
J	30-362007	A

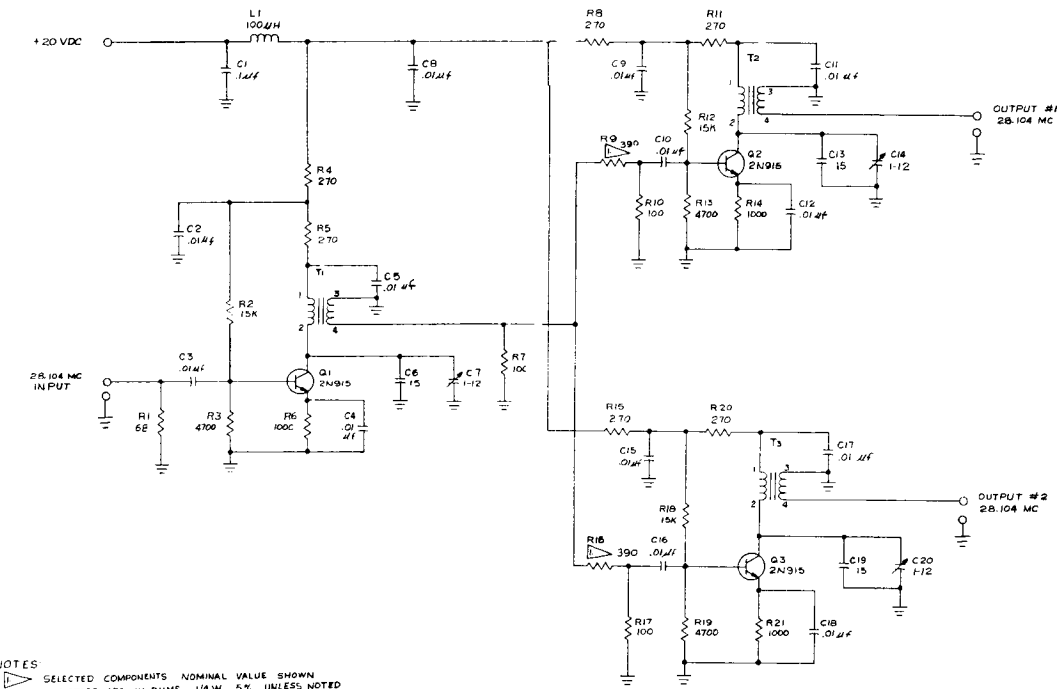
SCALE NONE



BLOCK DIAGRAM, ARGO TRANSPONDER RECEIVER

362034

A-02200



NOTES

1. SELECTED COMPONENTS NOMINAL VALUE SHOWN
2. ALL RESISTORS ARE IN OHMS 1/4 W 5% UNLESS NOTED
3. ALL CAPACITORS ARE IN PF UNLESS OTHERWISE NOTED

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

A-06123

362030	W0362	DRAWN	C. HORACK 17-DEC-63
PART NUMBER	USED ON	DATE	
APPLICATION		CHECKED	1-2-64
		DATE	
		APPROVED	
		DATE	

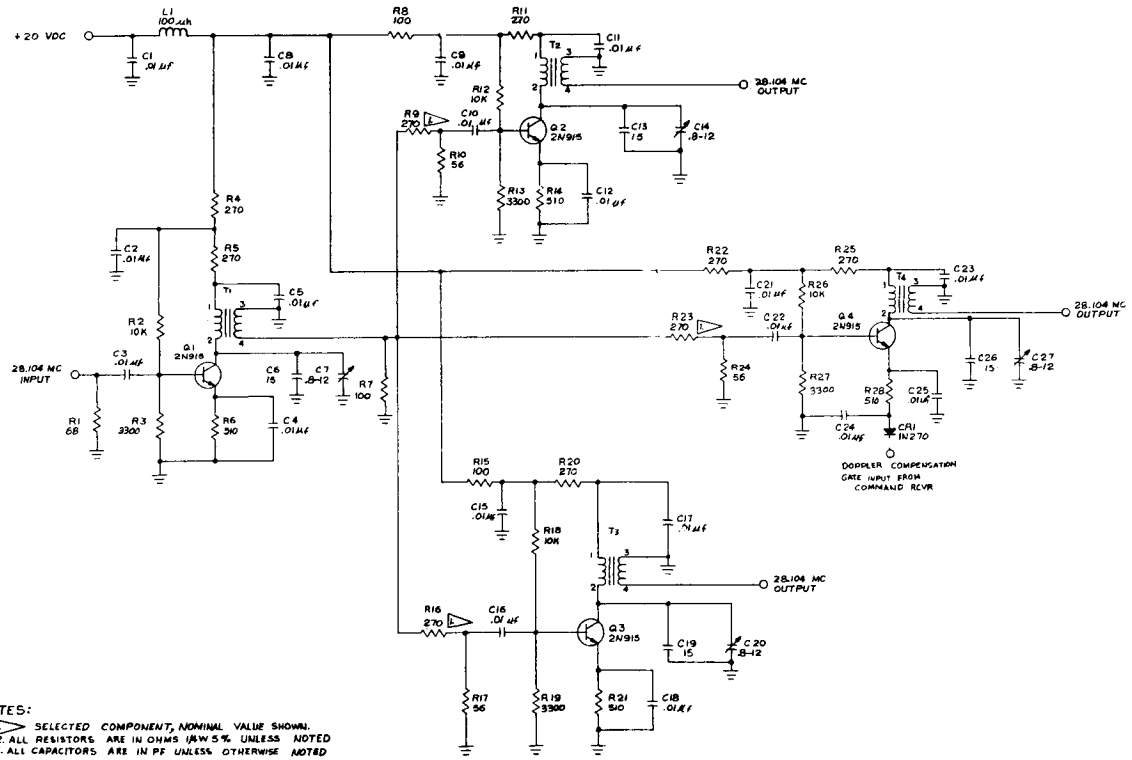
SCHEMATIC, TRACKING VCO ISOLATION AMPLIFIER

SCALE NONE SHT OF

Space Craft Inc. Huntsville, Ala.

SIZE D SCI-362028 SHEET OF

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL
A	CORRECTED		



NOTES:
1. SELECTED COMPONENT, NOMINAL VALUE SHOWN.
2. ALL RESISTORS ARE IN OHMS I/4W 5% UNLESS NOTED
3. ALL CAPACITORS ARE IN PF UNLESS OTHERWISE NOTED

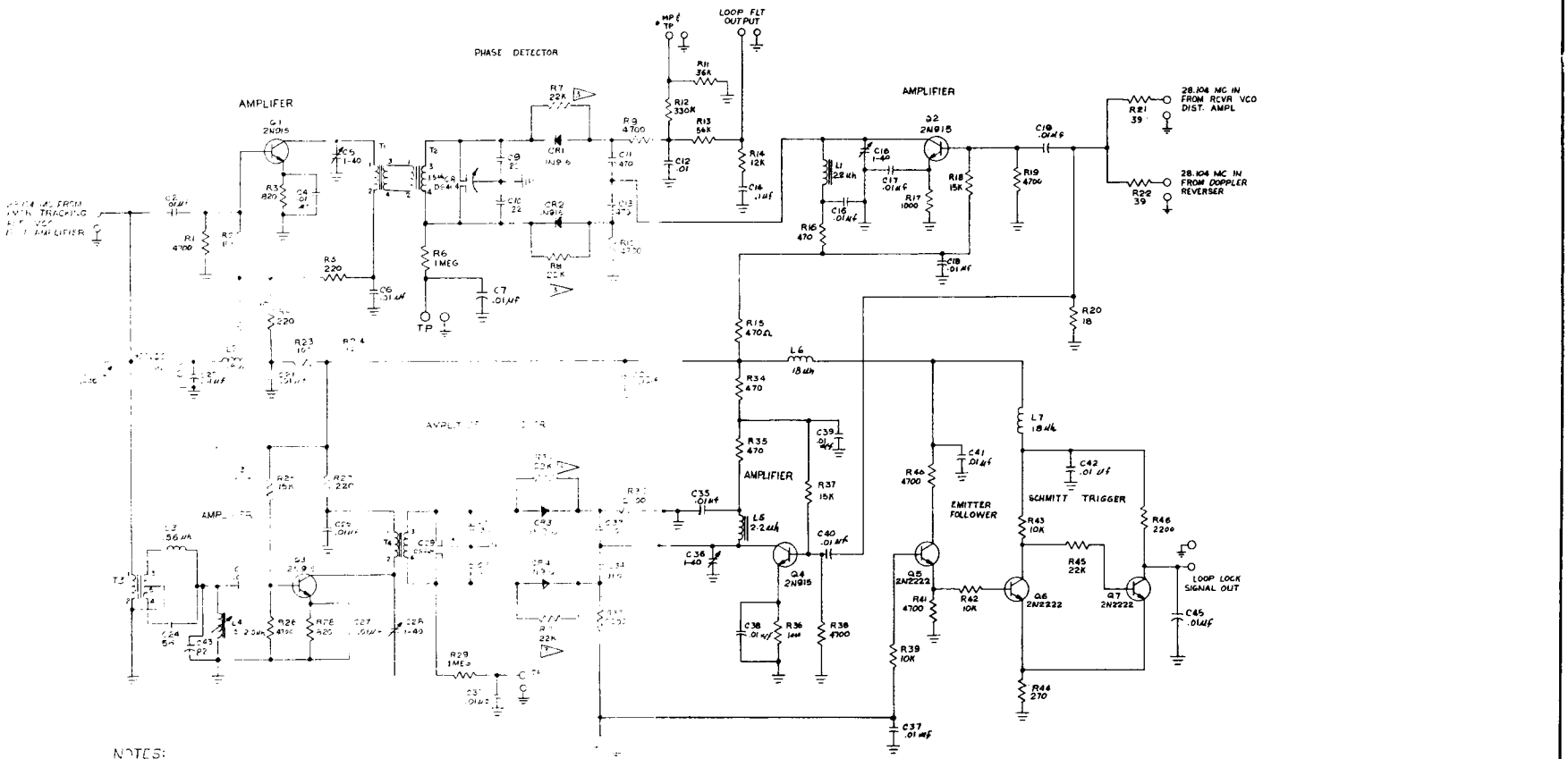
A-02252

362033	W0362	UNLESS OTHERWISE SPECIFIED	DRAWN	C. HORACE	SCHEMATIC, RECEIVER VCO DISTRIBUTION AMPLIFIER
			DATE	15-DEC-63	
			CHECKED	RE	
			DATE	1-2-64	
			APPROVED	TEG	
			DATE	1-23-64	
APPLICATION					SCALE NONE

Space Craft Inc.
Huntsville, Ala.

SIZE D | SCI-362031 | A

SHEET

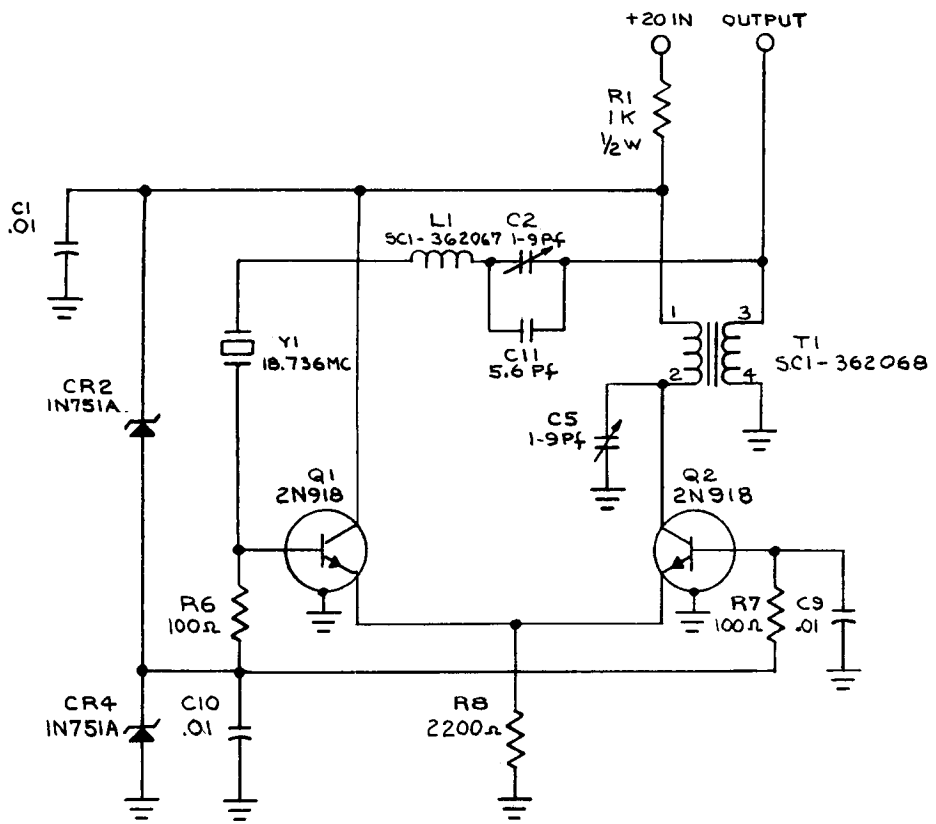


NOTES:
1. ALL RESISTORS ARE 1/4W 5%
2. ALL CAPACITORS 1 MF UNLESS OTHERWISE NOTED
3. SELECTED TO FIT
4. LAST REFERENCE DESIGNATIONS USED: C45; CR2; R46; Q7; L7; T4
5. REFERENCE DESIGNATION NOT USED: C44

A-06111

		C. Hornick	SCHEMATIC, TRACKING LOOP	Space Craft Inc. Huntsville, Ala.
		16-Dec-63		
		1-2-64		
362041	WO362		NONE	D SCI-362039

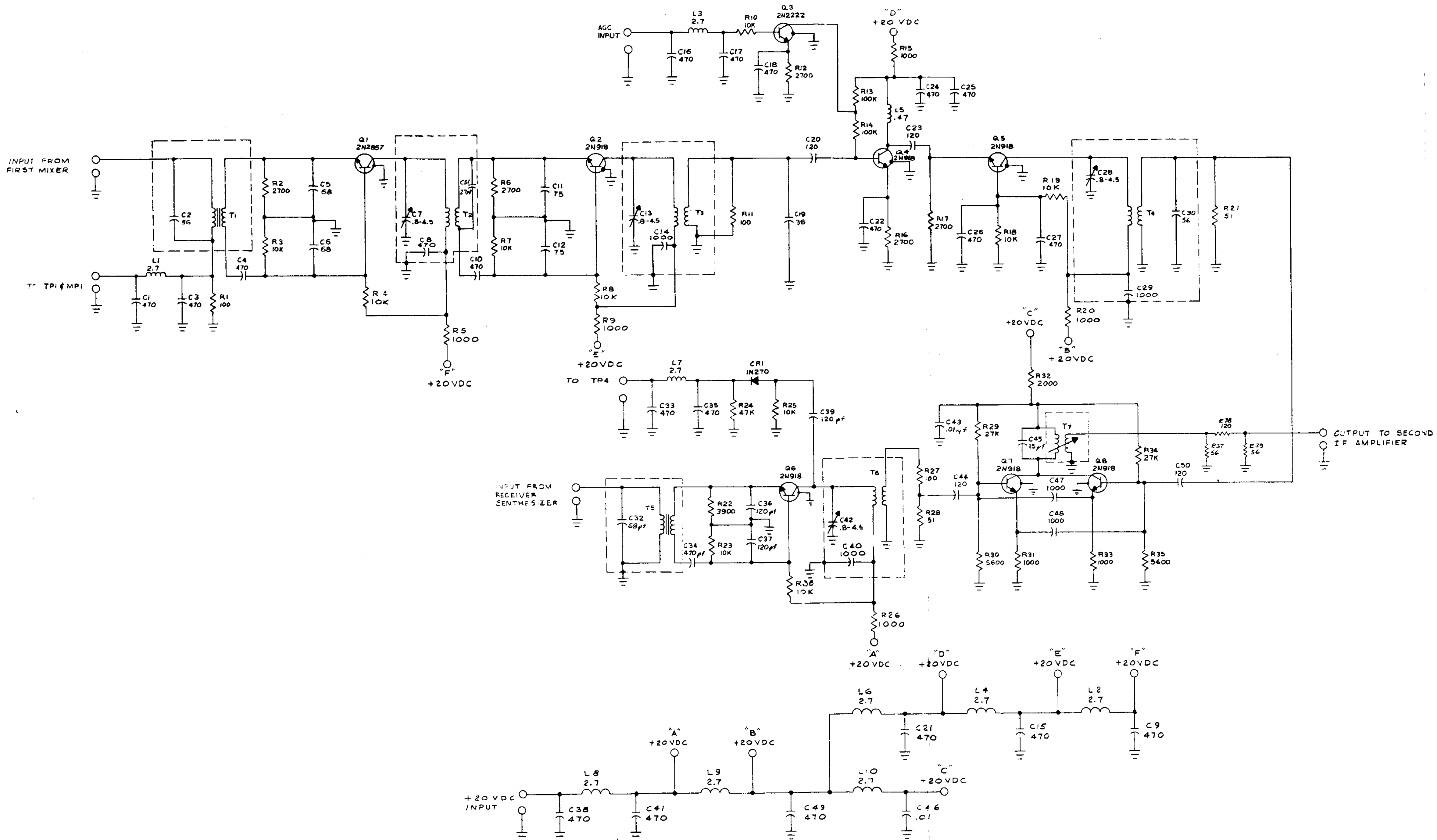
REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL



A-06122

		UNLESS OTHERWISE SPECIFIED	DRAWN	RR	SCHEMATIC, 18.73600 MC OSCILLATOR
		DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES	DATE	2-14-64	Space Craft Inc. Huntsville, Ala.
		MATERIAL	CHECKED	J.W.	
			DATE	2-14-64	
		HEAT TREATMENT	APPROVED		DWG. SIZE B — SCI-362048
D-362052	W.O. 362		DATE		
NEXT ASSY.	USED ON	FINAL PROTECTIVE FINISH			SCALE — UNIT WT. — SHEET OF
APPLICATION					

SYM	DESCRIPTION	DATE	APPROVAL
B	REVISED		



NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μμF
3. ALL INDUCTORS ARE IN μH
4. LAST REFERENCE DESIGNATIONS USED: R39, C51, CR1, T7, Q8, L10

4 0727

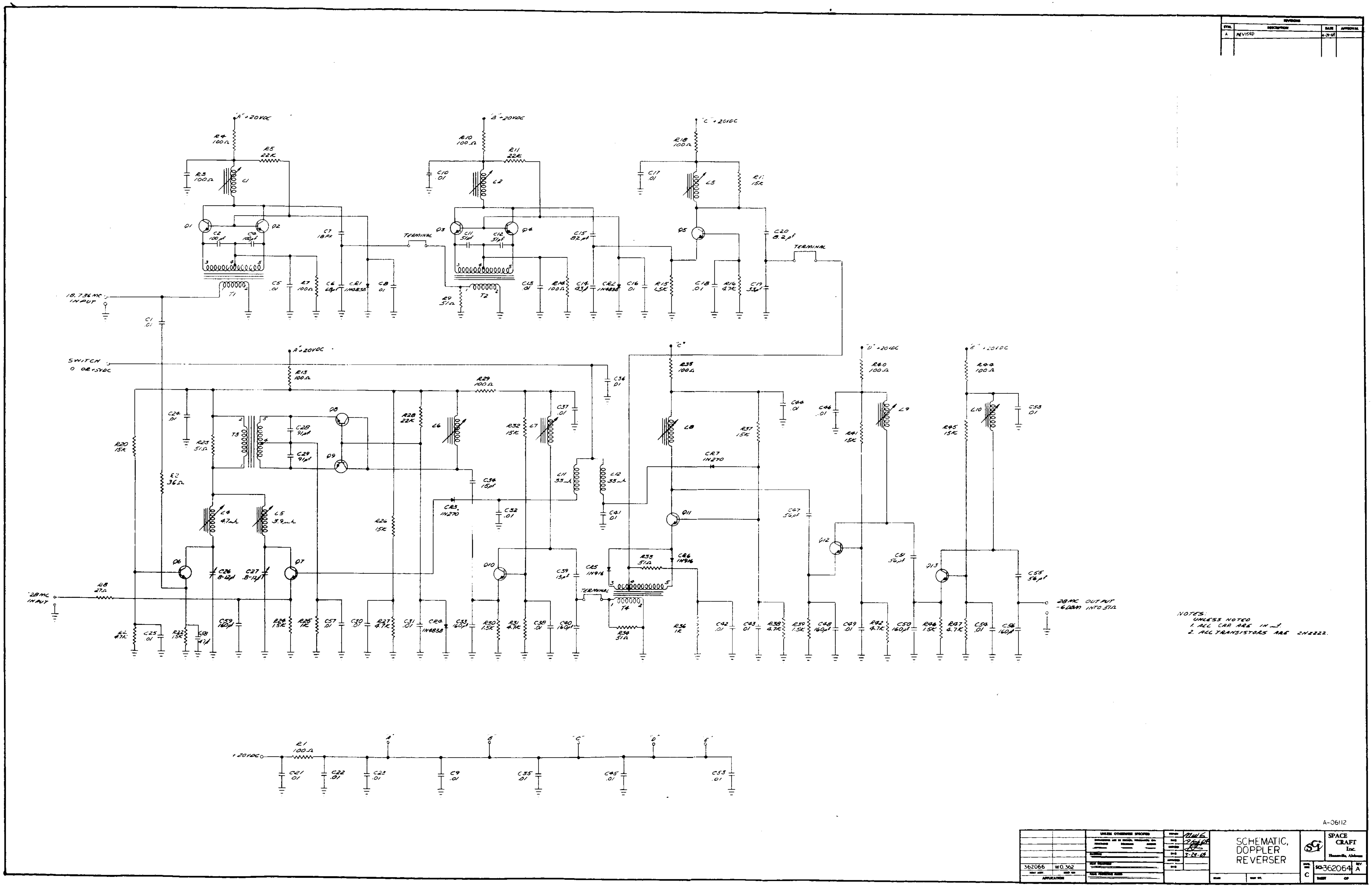
D362071	W0362
APPLICATION	

SCHEMATIC, 1st I.F. AMPLIFIER

Space Craft Inc. Huntsville, Ala.

SCI-362069 B

SCALE NONE


18.736 MC INPUT
SWITCH 0 OR +5VDC
28 MC INPUT
28 MC OUTPUT +6 DBM INTO 51Ω
TERMINAL
+20VDC
NOTES:
UNLESS NOTED
1. ALL CAP ARE IN µf
2. ALL TRANSISTORS ARE 2N2222.
SCHEMATIC, DOPPLER REVERSER
SPACE CRAFT Inc.
SD-362064
A-06112
362066 W.O. 362
A REVISED

SYM	DESCRIPTION	DATE	APPROVAL
A	REVISED	2-DEC	
B	REVISED	3 JAN	KB

MP11 TP38 (DC) TP39 (DC) TP40 (DC) MP12

TP2 AMP φ DET DC AMP SCHMITT TRIGGER

AMP 12 fo LOOP FILTER φ DET AMP

TRACKING LOOP 362040 A-06111

TP36 (DC) TP37 (DC) FROM AROD RECEIVER VCO

12 fo ± fo LINEAR ADDER

12 fo ± fo

DOPPLER REVERSER 362065 A-06112

AMP 12 fo - fo MIXER AMP 36 fo

20 fo + fo 20 fo MIXER AMP

X4 AMP 24 fo 4 fo SW 24 NOTE 2

4 fo

TRANSMITTER TRACKING FILTER A-0680

AMP 12 fo X4 X6

φ DET 12 fo LOOP FILTER VCO 1/2 AMP AMP

DIVIDE BY 24 LOOP 362010 A-06113

12 fo

MP13 TP41 (DC) 12 fo ± fo INPUT FROM COMMAND RCVR OR REC VCO TP42 (DC) TP43 (DC) TP44 (DC) TP45 (RF)

DOPPLER COMPENSATION GATE INPUT FROM COMMAND LOGIC

4 fo

TP46 (RF)

362012 Ref OSC Power Amp

362181 VCO 12 fo A-06131

REF OSC 8 fo 362013 362014 362022

TRACKING LOOP VCO DISTRIBUTION AMP 362023 A-06123

AMP AMP AMP

TP80 (RF)

12 fo 12 fo

TRACKING VCO AND REFERENCE OSCILLATOR A-06120

TP47 (DC) TP48 (DC) TP49 (DC) TP50 (RF)

PCO DRIVER PCO X 19 AMP φ DET 35 fo LOOP FILTER VCO 35 fo AMP X 3

X 57 MULTIPLIER LOOP 362163 A-0631

28.8 fo

TP 79 (VCO SWITCH)

TRANSMITTER SYNTHESIZER A-6170

X 60 MULTIPLIER LOOP 362032 A-6132

AMP X2 PCO DRIVER PCO X 120 AMP φ DET LOOP FILTER VCO 30 fo AMP AMP

TP 78 (VCO SWITCH)

30 fo

TP64 (DC) TP53 (DC) TP52 (DC) TP51 (RF)

TP55 (DC) TP56 (DC) TP57 (DC)

PCO DRIVER PCO X24 AMP φ DET 12 fo LOOP FILTER VCO 2.4 fo AMP AMP

X 4.8 MULTIPLIER LOOP CHANNEL 1 362130 A-06141

2.4 fo

TP58 (RF) MP14 TP59 (DC)

SPECTRUM GENERATOR #1 A-0616

X 6 MULTIPLIER LOOP CHANNEL 2 362130 A-06142

AMP X5 SW 5

1 CHANNEL 2 FREQUENCY SELECTION COMMAND INPUTS FROM COMMAND RCVR

MP15 TP60 (DC)

PCO DRIVER PCO X 30 AMP φ DET 15 fo LOOP FILTER VCO 3.0 fo AMP AMP

3 fo

TP63 (DC) TP62 (DC) TP61 (DC)

TP64 (DC) TP65 (DC) TP66 (DC)

PCO DRIVER PCO X53 AMP φ DET 265 fo LOOP FILTER VCO 5.3 fo AMP AMP

5.3 fo

TP67 (RF)

X 10.6 MULTIPLIER LOOP CHANNEL 3 362235 A-06131

AMP X5 SW 6

TP68 (DC) MP16

SPECTRUM GENERATOR #2 A-06160

X 11.8 MULTIPLIER LOOP CHANNEL 4 362135 A-06132

AMP X5 SW 4

3 CHANNELS 4 FREQUENCY SELECTION COMMAND INPUTS FROM COMMAND RCVR

MP17 TP69 (DC)

PCO DRIVER PCO X 59 AMP φ DET 295 fo LOOP FILTER VCO 5.9 fo AMP AMP

5.9 fo

TP72 (DC) TP71 (DC) TP70 (DC)

MP 19

AMP DET TRANSMITTER MIXER 362035 A-0617

NP18 2.4 fo OR 3.0 fo 5.3 fo OR 5.9 fo

LINEAR ADDER AMP BAL MIXER FILTER AMP

DET MP19A

TRANSMITTER MODULATOR A-06170

TP 74 (RF)

TP FC (RF)

LINEAR POWER AMPLIFIER 362178 A-06173

TP 75 (RF)

LINEAR ADDER LINEAR AMP LINEAR AMP LINEAR POWER AMP DET

AMP AMP GATED Φ TRIMMER GATED Φ TRIMMER

TP82 TP81 TP84 TP83

0 CHANNEL 1 CHANNEL 2 CHANNEL 3 CHANNEL 4

CHANNEL SELECTION COMMAND INPUTS FROM COMMAND LOGIC

LOW FREQ I INFORMATION FILTER

LINEAR ADDER LINEAR AMP BAL MIXER LINEAR ADDER LINEAR ADDER

÷2 ÷2 AMP

SIMPLEX L BAND SYNTHESIZER 362178 A-06173

2.2088 MC 2.342 MC

FROM AROD RECEIVER RANGE TONE CIRCUITS

TP73 (DC) MP20

ATTEN A-06199

TRANSMITTER L BAND MIXER A-06180 MIXER 312 fo

324.6 fo 332.0 fo 337.1 fo 337.9 fo

"S" BAND RF OUTPUT

NOTES:
1. SWITCHES SHOWN IN LOGIC 0 POSITION
2. SWITCH 2A LOCATED IN AROD RECEIVER
3. MONITOR POINTS:
   - MP11 TRANSMITTER TRACKING LOOP DET. OUTPUT
   - MP12 TRANSMITTER TRACKING LOOP LOCK INDICATION
   - MP13 DOPPLER COMPENSATION GATE INPUT
   - MP14 X 4.8 LOOP SELECTOR SWITCH INPUT
   - MP15 X 6 LOOP SELECTOR SWITCH INPUT
   - MP16 X 10.6 LOOP SELECTOR SWITCH INPUT
   - MP17 X 11.8 LOOP SELECTOR SWITCH INPUT
   - MP18 XMTR MODULATOR BAL MIXER INPUT (FROM SPECTRUM GENERATOR #1)
   - MP19 XMTR MODULATOR BAL MIXER INPUT (30 fo)
   - MP20 XMTR MODULATOR OUTPUT
   - MP19A XMTR MODULATOR BAL MIXER INPUT (FROM SPECTRUM GENERATOR #2).
4. fo = 2.342 MC. ; fo = DOPPLER SHIFT ON 12 fo

APPLICATION: WO362	DRAWN: C. HORACE 5-DEC-63	BLOCK DIAGRAM, AROD TRANSPONDER EXCITER	Space Craft Inc. Huntsville, Ala.
	ENGR: [illegible] 12-6-63		SIZE J SCI 362042
	APPROVED: [illegible] 12-11-63		
	MFG APPR: NONE		

NO.	DESCRIPTION	DATE	APPROVED
A	REDRAWN	1-17-68	

NOTES
1. ALL CAPACITORS IN PF UNLESS NOTED.
2. ALL RESISTORS IN OHMS 1/4W 5% UNLESS NOTED.
3. ALL INDUCTORS IN μH UNLESS NOTED.
4. LAST REFERENCE DESIGNATIONS USED: R44, C68, CR4, Q7, L15, T1, Y1

A-02263

SCHEMATIC DIVIDE BY 24 LOOP			
362011	W0362	NONE	362009 A

REVISIONS			
NO.	DESCRIPTION	DATE	APPROVAL
4	ECN 1560		

-20VDC INPUT

C44 .47μf
L11 110
C45 .47μf
R9 10K
C6 .1μf
R8 12K
R6 1MEG
R4 1MEG
R1 1MEG
CR2 FC 116
CR1 FC 116
C4 .1μf
C8 68
Y1 2.268812 MC
L8 270
2.268812 MC VCO
L1 225-390
C9 51
T1
C5 330
C3 1-40
Q1 2N918
C1 .1μf
R2 1500
C2 .1μf
R10 3.9K
R7 1500
R5 10K
R3 3300
C7 .47
+20 VDC "A"
CR11 IN270
RANGE TONE GATE INPUT
C49 0.1μf
+20 VDC "B"
R37 750K
C26 .1μf
R36 150K
+20VDC "D"

OUTPUT AMPLIFIER
R19 10K
R20 3900K
Q3 2N718
C20 .1μf
C21 270
C22 1-40
T4
2.268 MC OUTPUT
R21 1000
R22 470
C23 .47μf
+20 VDC "C"

TP
C14 .1μf
PHASE DETECTOR
R14 1MEG
R15 2.2K
R18 3300
CR3 IN916
C17 1000
C15 75
C47 DS464
C48 10
T3
T2
C18 1000
C16 75
CR4 IN916
REFERENCE AMPLIFIER
C13 1-40
C11 270
Q2 2N718
R12 820
C10 .1μf
R13 330
C12 .47μf
R11 10K
+20 VDC "B"
TP
C19 .01μf
R17 3300
R16 2.2K
R47 330K
MP
R48 36K

R30 1000
R25 100K
R53 100K
Q6 2N2907
Q10 2N2907
Q7 2N929
Q8 2N929
Q4 2N929
R26 100K
R34 100K
C24 .C2
R27 10K 1%
C5A 2N2453
CR5 IN751
C58 2N2453
R35 10K 1%
C25 .C2 4f
R32 511 1%
R28 511 1%
R24 750K
CR6 IN751
NC
DC AMPLIFIER
Q9 2N718
Q13 5439
R23 10K
R52 100Ω
R31 5000
R29 7500
CR7 IN751
C46 .47μf
TP

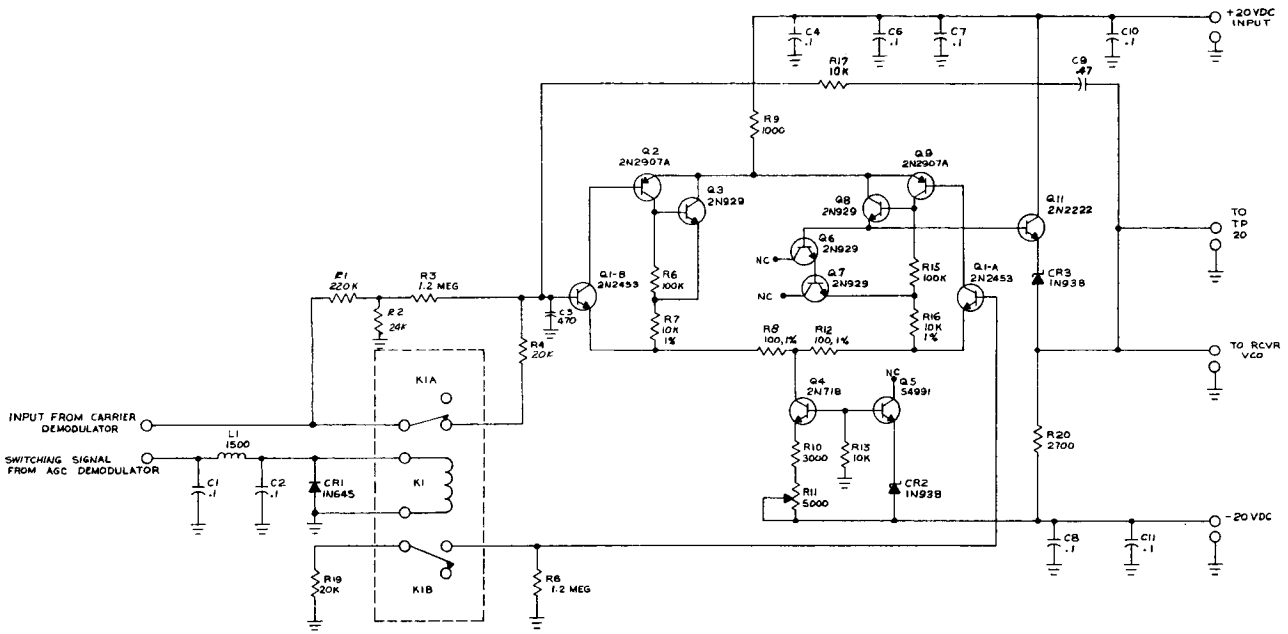
R50 4300
SIGNAL AMPLIFIER & LIMITER
Q11 2N718
C32 .1
Q12 2N718
C33 360
C35 1-40
R51 1000
L2
R53 100
C27 .1μf
C28 2.40
C30 1-40
T5
R49 56
2.268 MC INPUT
CR9 IN916
CR10 IN916
R46 680
C36 .47μf
L10 33
R38 200
R39 3900
R40 1000
C29 .1μf
C31 .47
C34 .1μf
R42 100
R44 1000
R43 3300
R45 10K
R41 10K
+20 VDC "E"
+20 VDC "F"

+20VDC INPUT
+20 VDC "A"
+20 VDC "B"
+20VDC "C"
L3 100
L4 100
L6 100
L5 100
L8 100
C39 .47μf
+20VDC "E"
+20VDC "D"
C43 .47μf
C42 .47μf
C41 .47μf
C40 .47μf
L7 100
L9 100
C37 .47μf
C38 .47μf
C50 .47μf
+20VDC "F"

NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS ¼W. 5%
2. ALL CAPACITORS ARE IN pf
3. ALL INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED: R53, C50, CR11, L11, Y1, Q13, T5
5. REFERENCE DESIGNATIONS NOT USED: CR8

A-02242

DRAWN	Wilbanks	SCHEMATIC, 2.2688 MC RANGE TONE LOOP	Space Craft Inc. Huntsville, Ala.
DATE	22-DEC-67		
CHECKED	[illegible]		
DATE	12-27-67		
APPROVED	TEG		
DATE	3-5-68		
362017 / WO 362		SIZE J	SC-362016A
NEXT ASSY	USED ON	NEXT MFG.	SHEET OF
APPLICATION		mat'l NONE	



NOTES:
UNLESS OTHERWISE NOTED.
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μf
3. ALL INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED: R21, C11, CR3, Q11, L5, K1,
5. REFERENCE DESIGNATION NOT USED: C5, L2, L3, L4, L5, E21

A-02253

D-362084 W0362

SCHEMATIC, MAIN LOOP FILTER

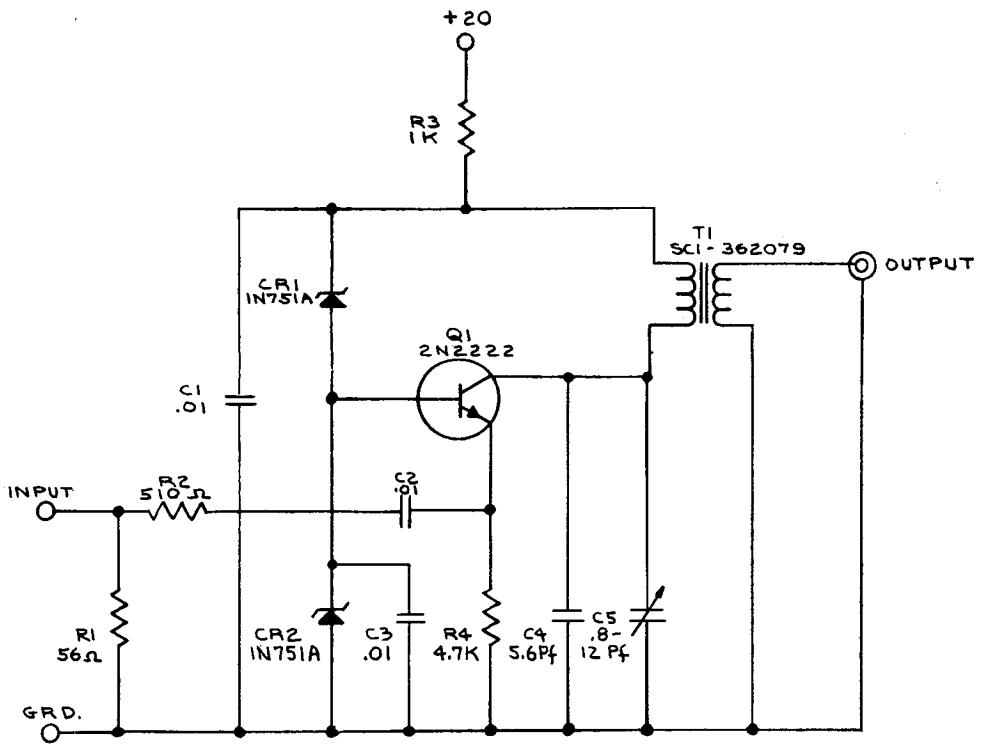
Space Craft Inc. Huntsville, Ala.

SCI-362082

D

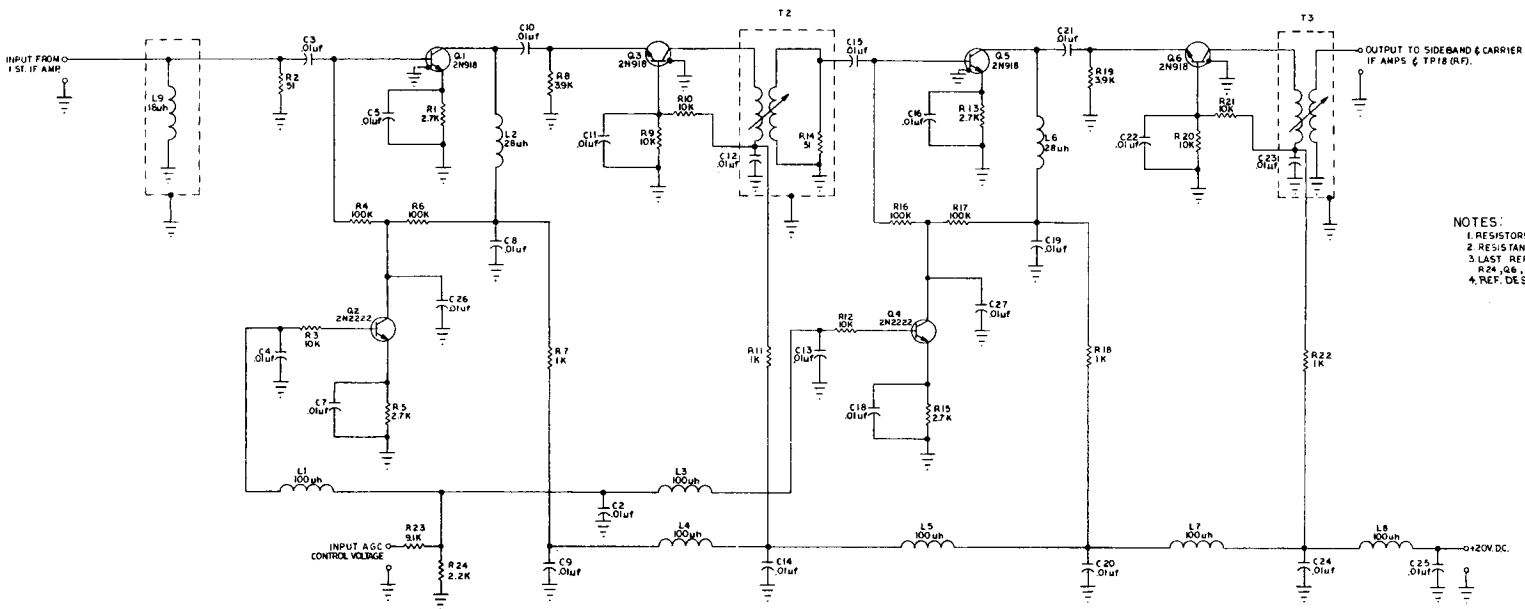
NONE

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL



A-06124

		UNLESS OTHERWISE SPECIFIED	DRAWN	RR	SCHEMATIC, REF. OSCILLATOR BUFFER	Space Craft Inc. Huntsville, Ala.	
		DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES	DATE	2-19-64			
			CHECKED	J.W.			
		MATERIAL	DATE	2-14-64			
			APPROVED				
		HEAT TREATMENT	DATE			DWG. SIZE B	SCI-362072
D-362074	WO 362						
NEXT ASSY.	USED ON	FINAL PROTECTIVE FINISH			SCALE	UNIT WT.	SHEET OF
APPLICATION							



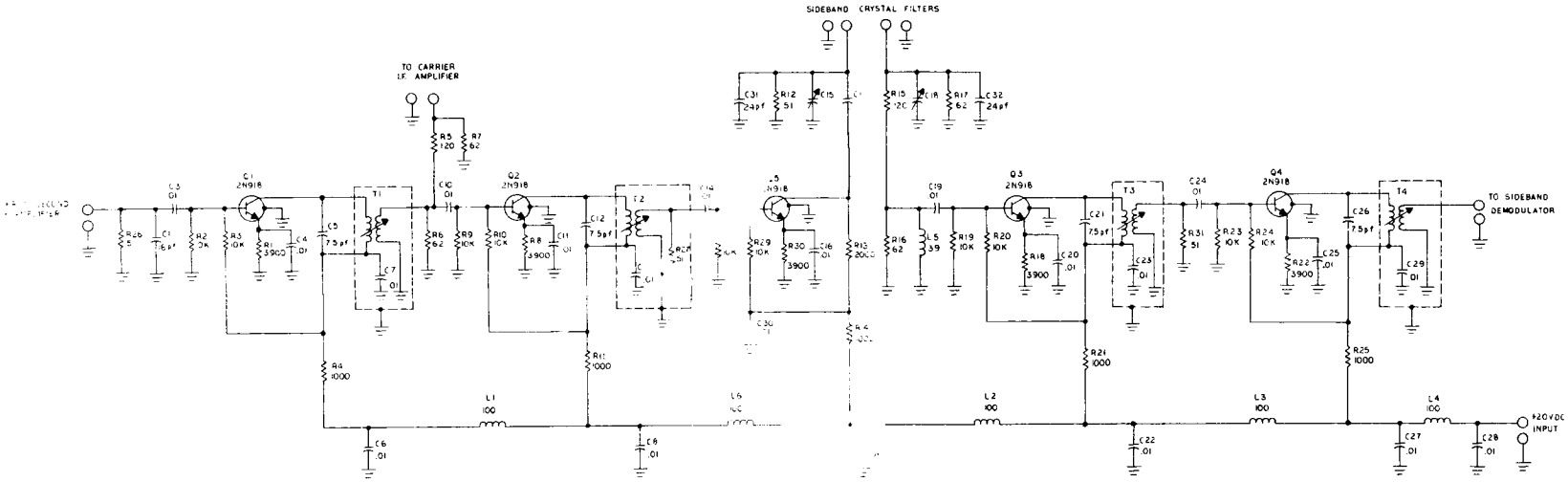
NOTES:
1. RESISTORS ARE 1/4W, 5%.
2. RESISTANCE VALUES IN OHMS.
3. LAST REFERENCE DESIGNATORS USED ARE: R24, Q6, T3, L9, C25.
4. REF. DES. NOT USED: C1, C6, C7, T.

A-02213

SCI-362090	W0-362	DRAWN	J.G. Hawley	SCHEMATIC, 2ND IF AMPLIFIER
		DATE	21-Feb-64	
		CHECKED	[illegible]	
		DATE	2-27-64	
		APPROVED	[illegible]	
		DATE	3/4/64	

Space Craft Inc. Huntsville, Ala.

SIZE D | SCI-362088 | SHEET | OF



NOTES:
1. UNLESS OTHERWISE NOTED
   RESISTORS ARE IN OHMS 1/4W 5%
2. CAPACITORS ARE IN μf
3. INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED
   R30, C32, L6, Q5
5. REFERENCE DESIGNATIONS NOT USED
   C2

A-02221

D-362102	W0362

DRAWN	C. HORACE
DATE	3-MARCH-64
CHECKED	
DATE	3-4-64
APPROVED	
DATE	4/4/64

SCHEMATIC, SIDEBAND I.F. AMPLIFIER

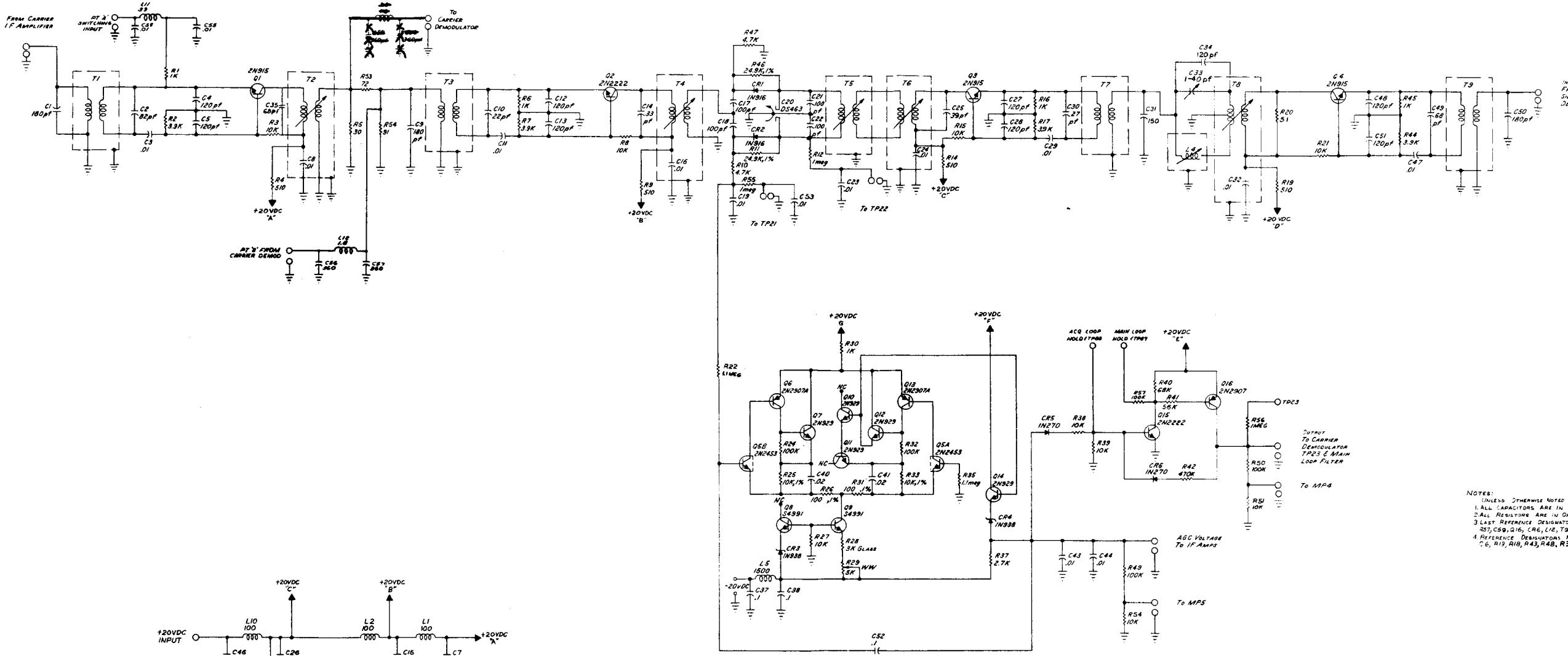
SCALE NONE

Space Craft Inc.
Huntsville, Ala.

SCI-362100

SIZE D

REVISIONS			
NO.	DESCRIPTION	DATE	APPROVED

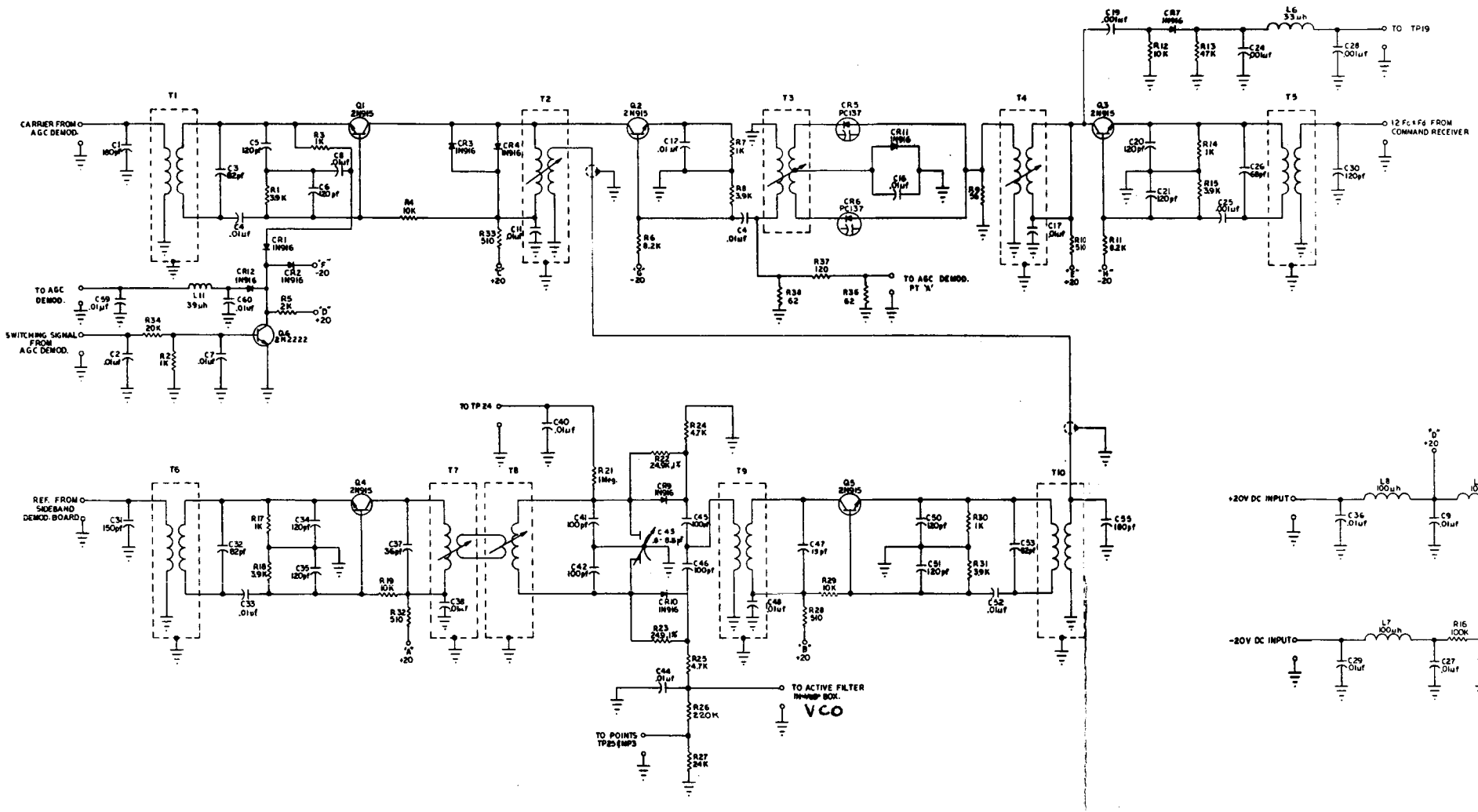


NOTES:
UNLESS OTHERWISE NOTED
1. ALL CAPACITORS ARE IN μF
2. ALL RESISTORS ARE IN OHMS 1/4W 5%
3. LAST REFERENCE DESIGNATORS USED: Z57, C59, Q16, CR6, L12, T9
4. REFERENCE DESIGNATORS NOT USED C6, R17, R18, R43, R48, R36, L7

A-02233

			E.E.G.	SCHEMATIC AGC DEMODULATOR	Space Craft Inc. Huntsville, Ala.
			10 Oct 64		
			1-4-65		
			W. Cheek		
0-362101	WO 362		4/4/65		SCI-362108
APPLICATION					J

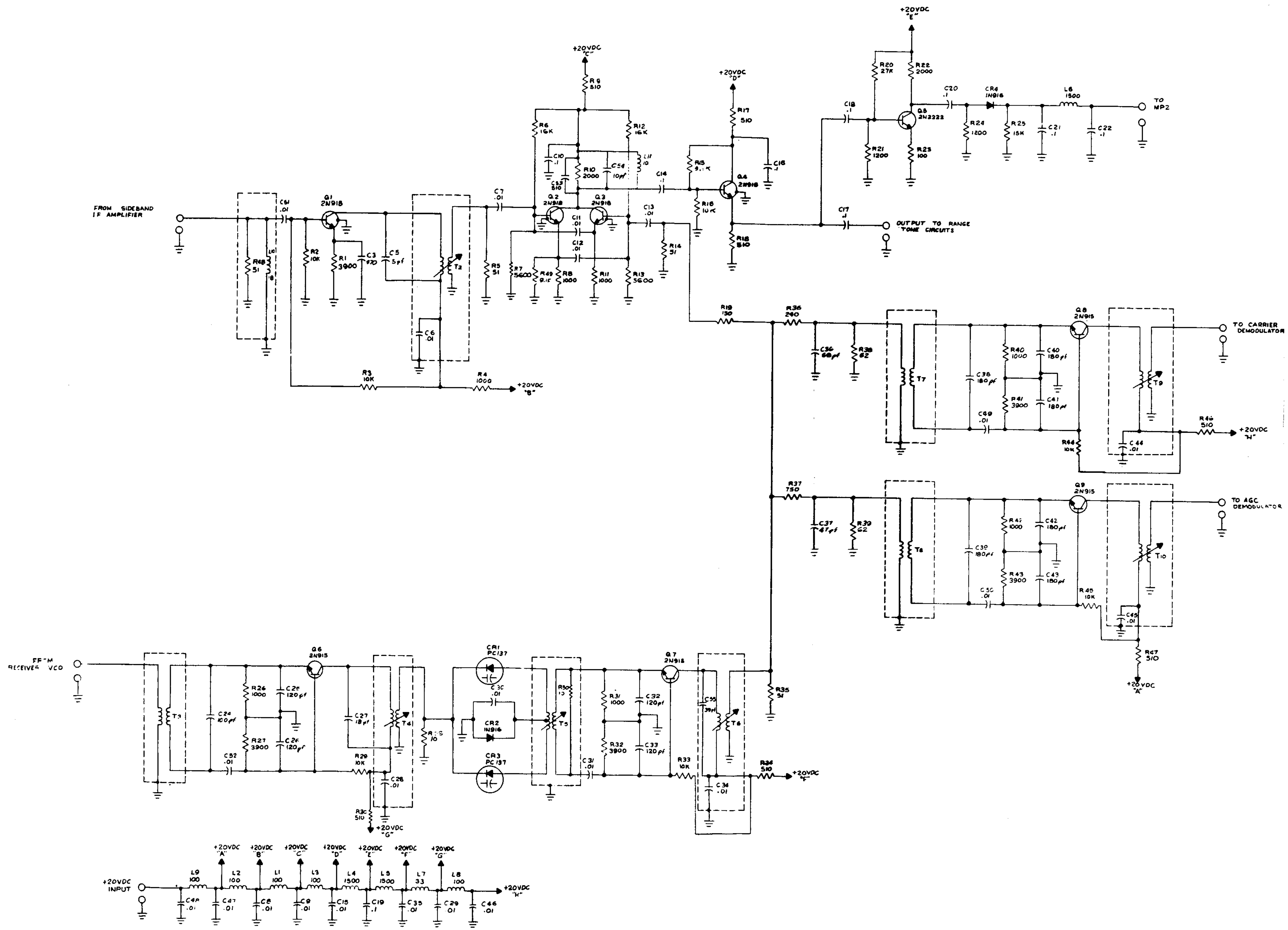
REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL



NOTES, UNLESS SPECIFIED:
1. RESISTORS ARE 1/4 W, 5%.
2. RESISTANCE VALUES IN OHMS.
3. LAST REFERENCE DESIGNATORS ARE: C60, R38, L11, Q5, T8, CR12.
4. REFERENCE DESIGNATORS NOT USED ARE: R20, C22, C36, C13, C58

A-02232

D-362087	W0-362	UNLESS OTHERWISE SPECIFIED	DRAWN	J.E. Mahaffey	SCHEMATIC, CARRIER DEMODULATOR	Space Craft Inc. Huntsville, Ala.
APPLICATION			DATE	20-Apr-67		
			ENGINEER			SIZE D	SCI-362085
			DATE	2-21-68		SHEET OF
			APPROVED			
			DATE			



NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITOR ARE IN μf
3. ALL INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED: R49, C55, T10, Q9, L10
5. REFERENCE DESIGNATIONS NOT USED: C1, C2, C4, C23, T1

A-02231

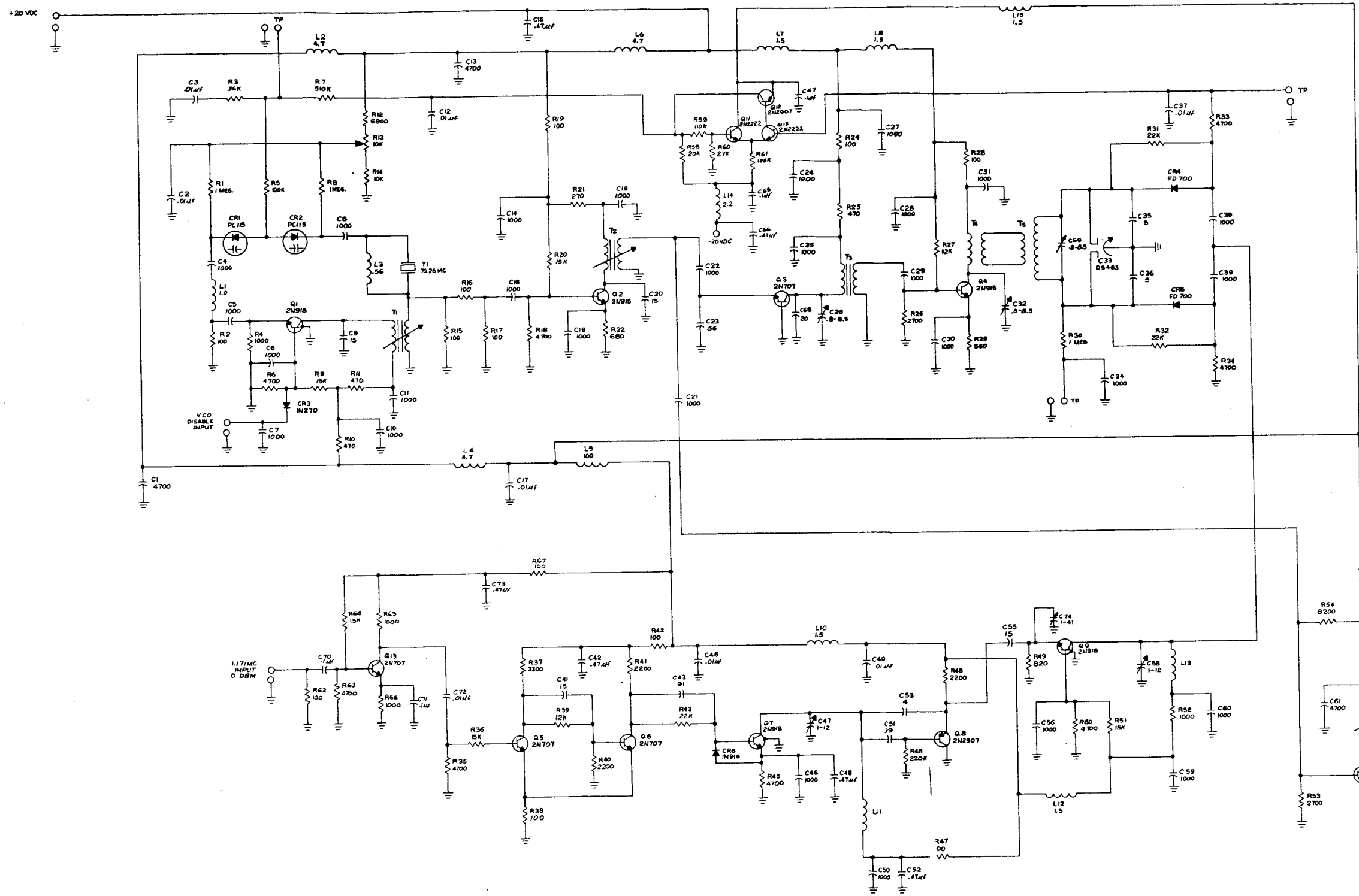
SCHEMATIC, SIDEBAND DEMODULATOR

Space Craft Inc. Huntsville, Ala.

D362077 | W0362

SCALE NONE

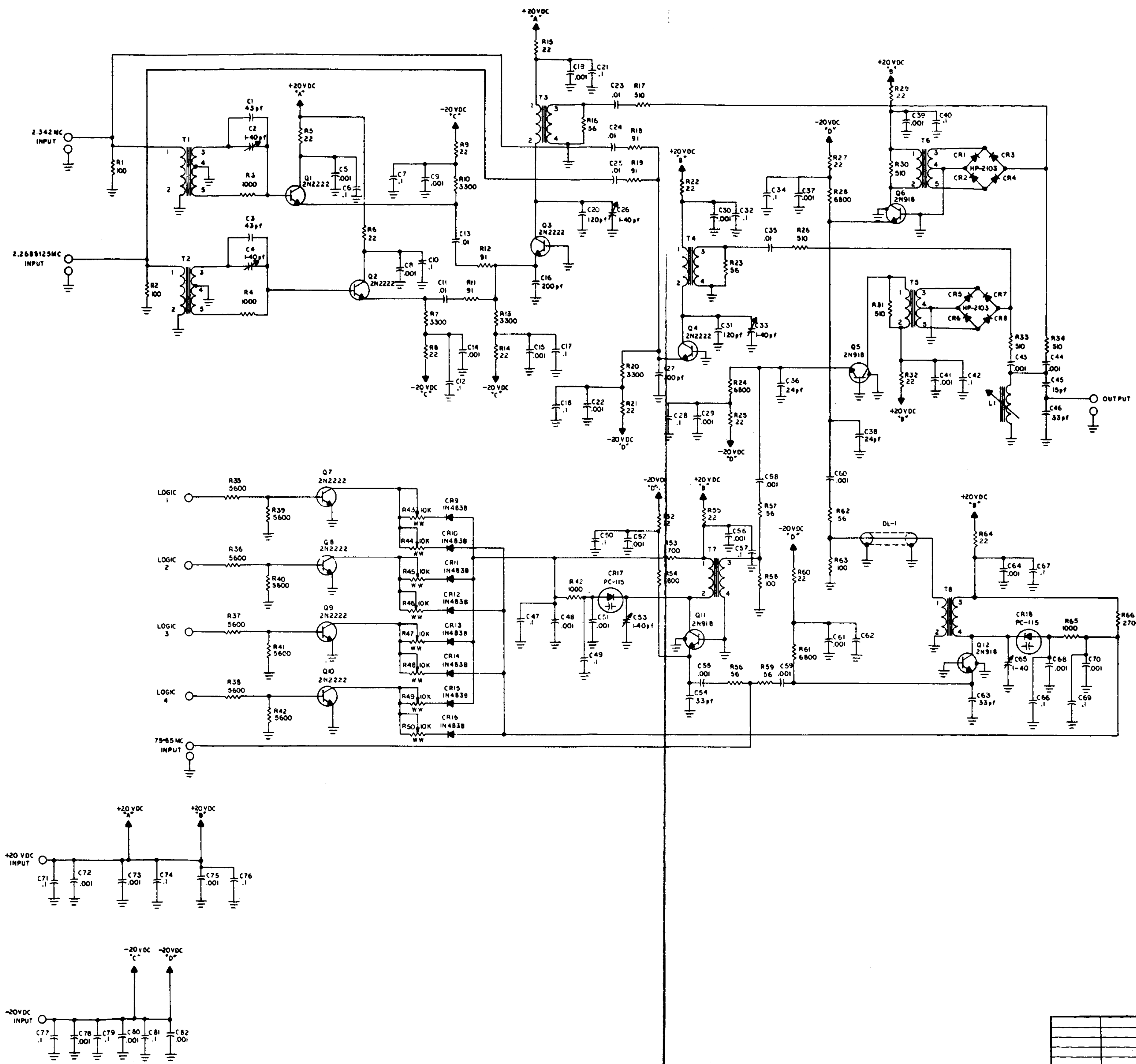
J | SCI-362075



NOTES:
1. ALL RESISTORS ARE 1/4W 5%
2. ALL CAPACITORS IN μF UNLESS NOTED.
3. ALL INDUCTORS IN μH UNLESS NOTED
4. LAST REFERENCE DESIGNATIONS USED R66, C74, CR6, L15, T6, Q13
5. REFERENCE DESIGNATIONS NOT USED C40, C44, C54, C57, R23, R44

A-06132

362093	W0362	C. Hankins 12-Nov-64	SCHEMATIC, X60 MULTIPLIER LOOP	Space Craft Inc. Huntsville, Ala.	
			NONE	D	SCI-362091



NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μf
3. INDUCTOR IN μh
4. LAST REFERENCE DESIGNATORS USED:
C82, CR18, L1, Q12, R66, T8, DL-1

A	REVISED	4-20	

SCHEMATIC
SIDEBAND GENERATOR

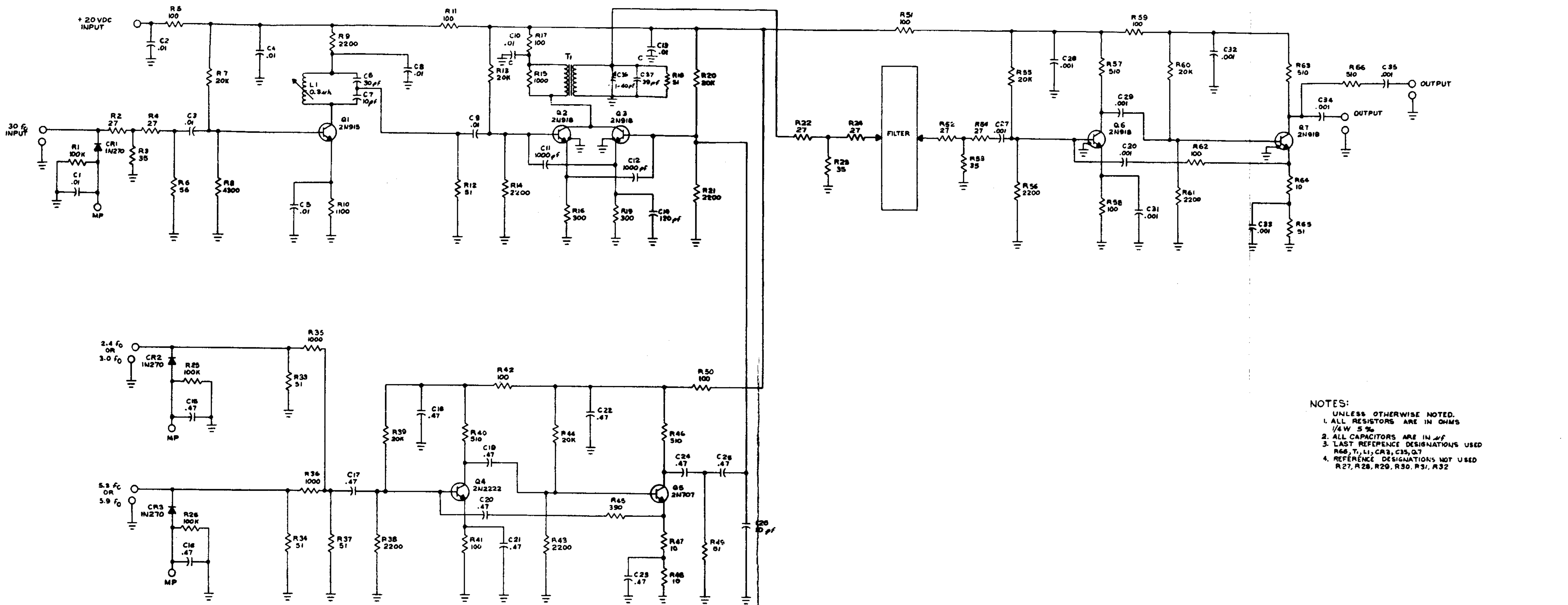
Space Craft Inc.

C. HORACE
9-MARCH-64
3-16-64

D362096 W0362

SCALE NONE

E SCI-362094 A



NOTES:
UNLESS OTHERWISE NOTED.
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN µf
3. LAST REFERENCE DESIGNATIONS USED R66, T1, L1, CR3, C35, Q7
4. REFERENCE DESIGNATIONS NOT USED R27, R28, R29, R30, R31, R32

A-C271

D 362097	WO 362

SCHEMATIC,
TRANSMITTER MIXER

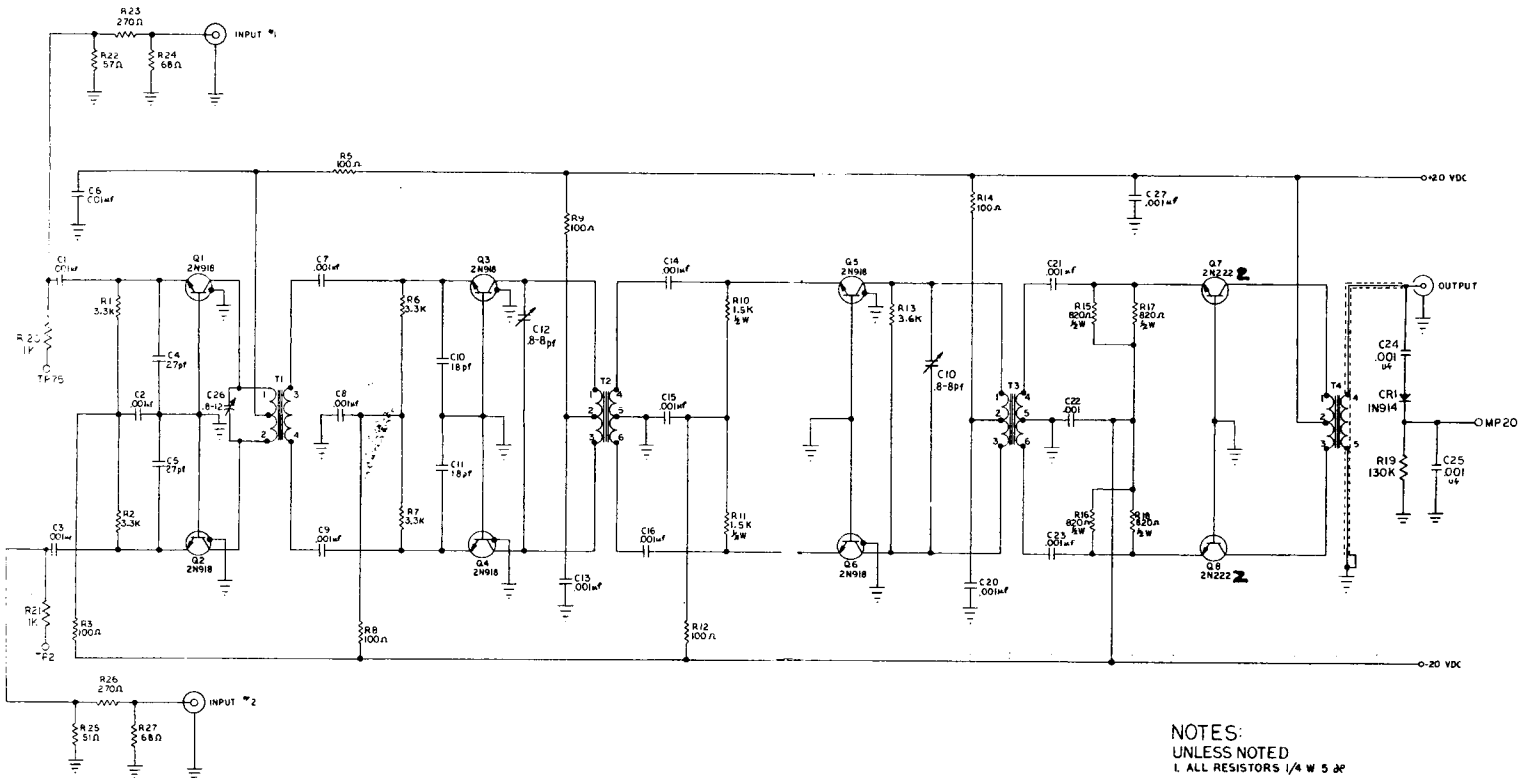
Space Craft Inc.
Huntsville, Ala.

SCALE NONE

J

SCI-362097

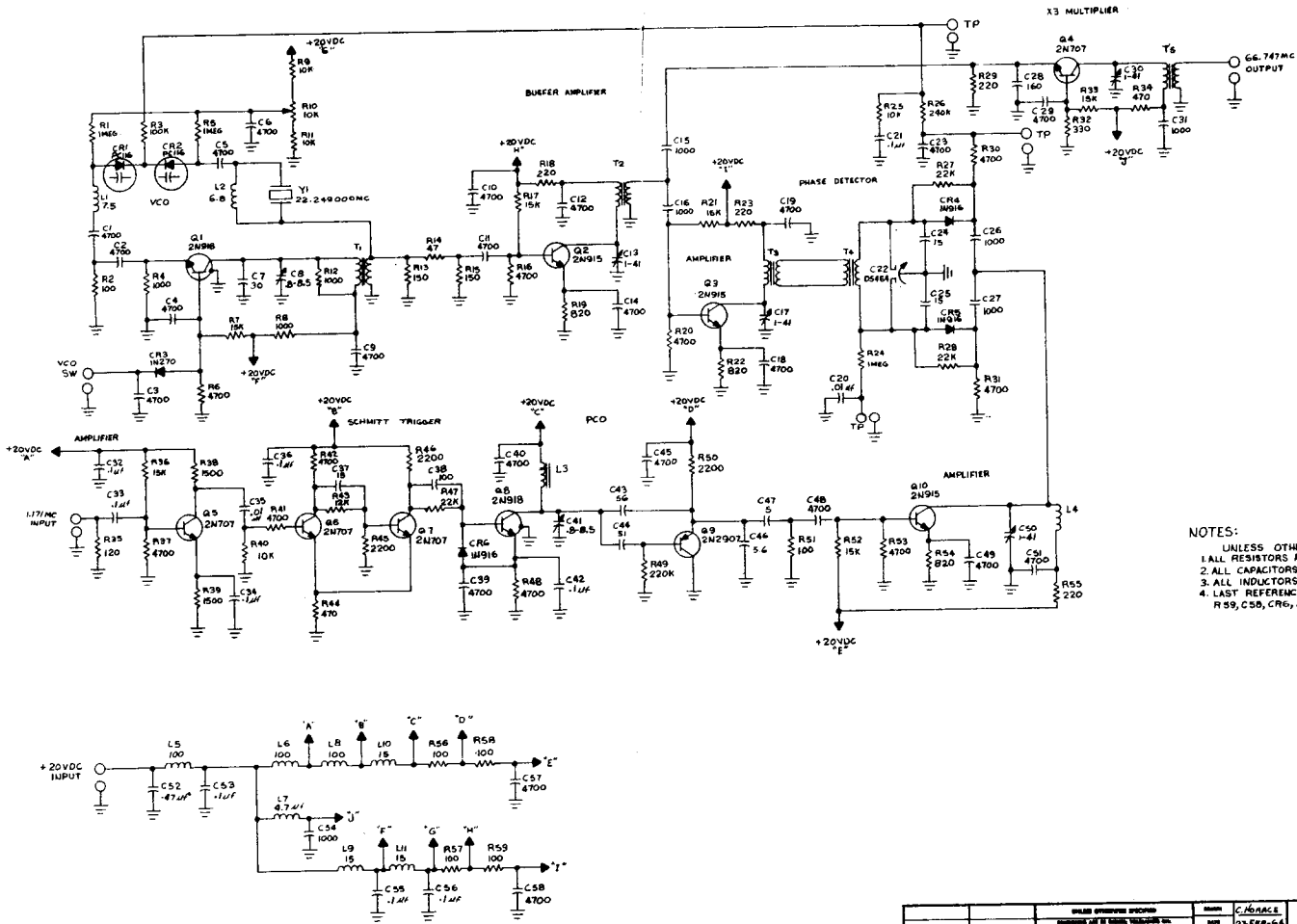
SYM	DESCRIPTION	DATE	APPROVAL
A	REVISED	4-20-64	



NOTES:
UNLESS NOTED
1. ALL RESISTORS 1/4 W 5 %

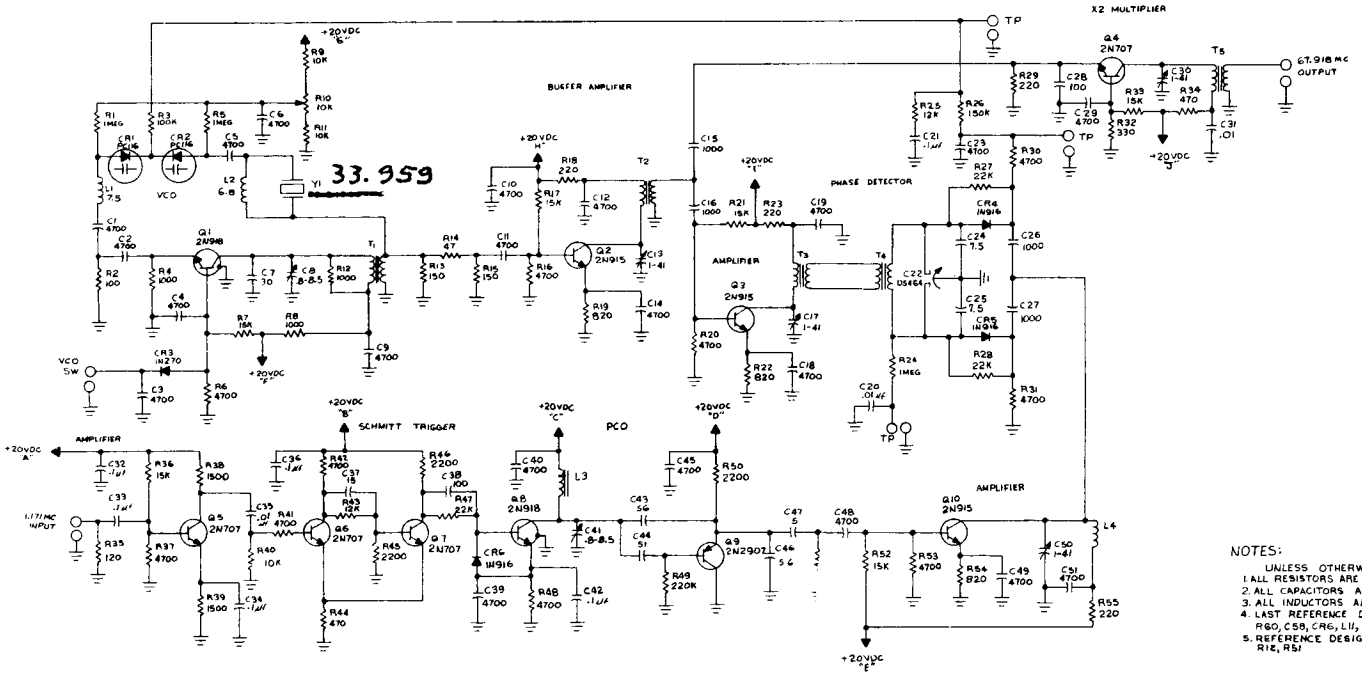
A-06173

0362115	WO-362			SCHEMATIC; 75-85MC POWER AMPLIFIER	Space Craft Inc. Huntsville, Ala.
					SCI-362113 A
					D



A-06131

D362140 W0362	C. HORACE	SCHEMATIC, X57 MULTIPLIER	Space Craft Inc. Huntsville, Ala.
	27-FEB-64		
	3-17-64		SCI-362139
		NONE	D



NOTES:

UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μf
3. ALL INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED R60, C58, CR6, L11, Q10, T5, Y1
5. REFERENCE DESIGNATORS NOT USED: R1E, R5I

A-02261

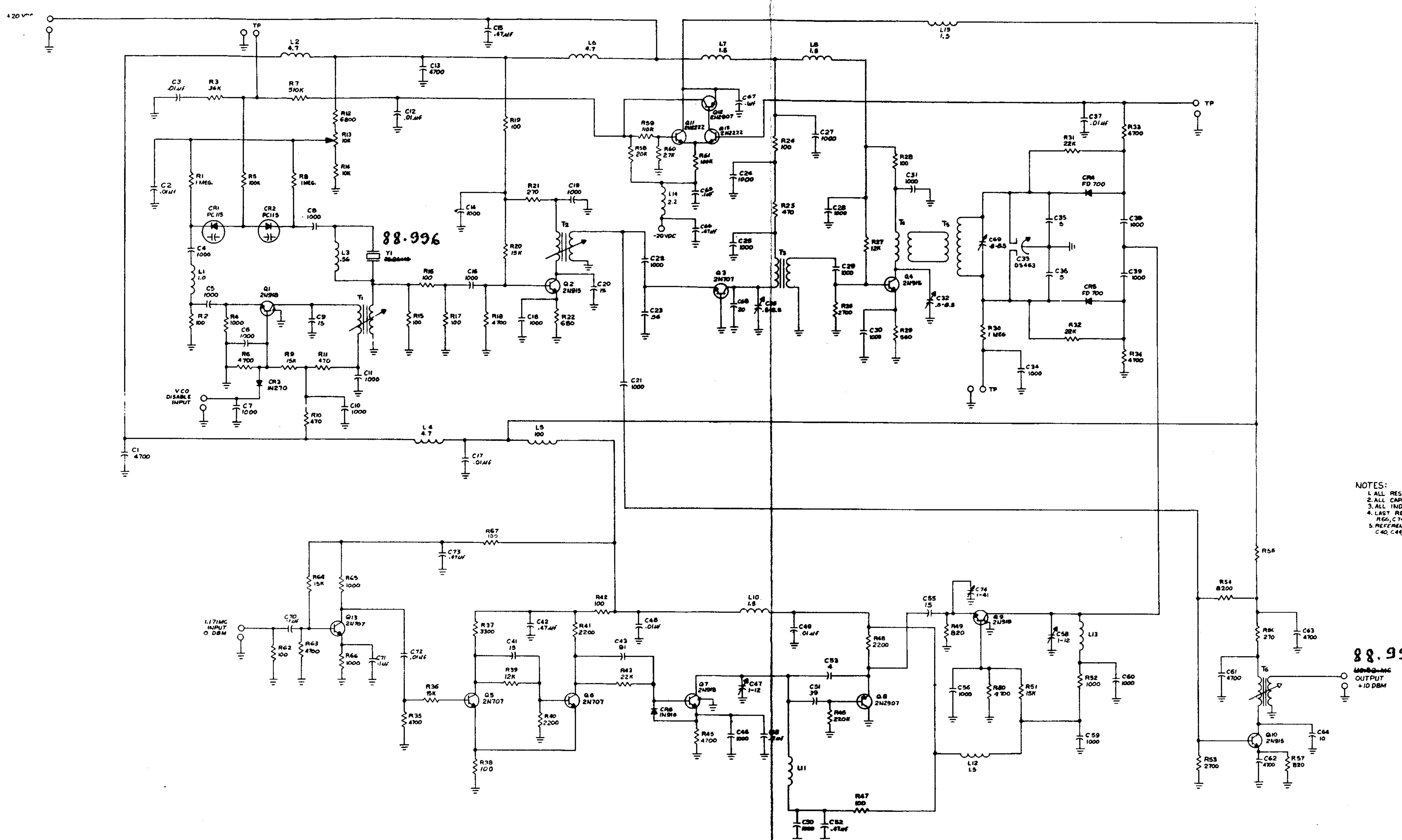
0362142	W0362	DRAWN	C. Mobley
		DATE	17-MAR-64
		CHECKED	
		DATE	3/18/64
		APPROVED	
		DATE	

SCHEMATIC, X58 MULTIPLIER

NONE

Space Craft Inc. Huntsville, Ala.

SIZE D | SCI-362141 | SHEET OF



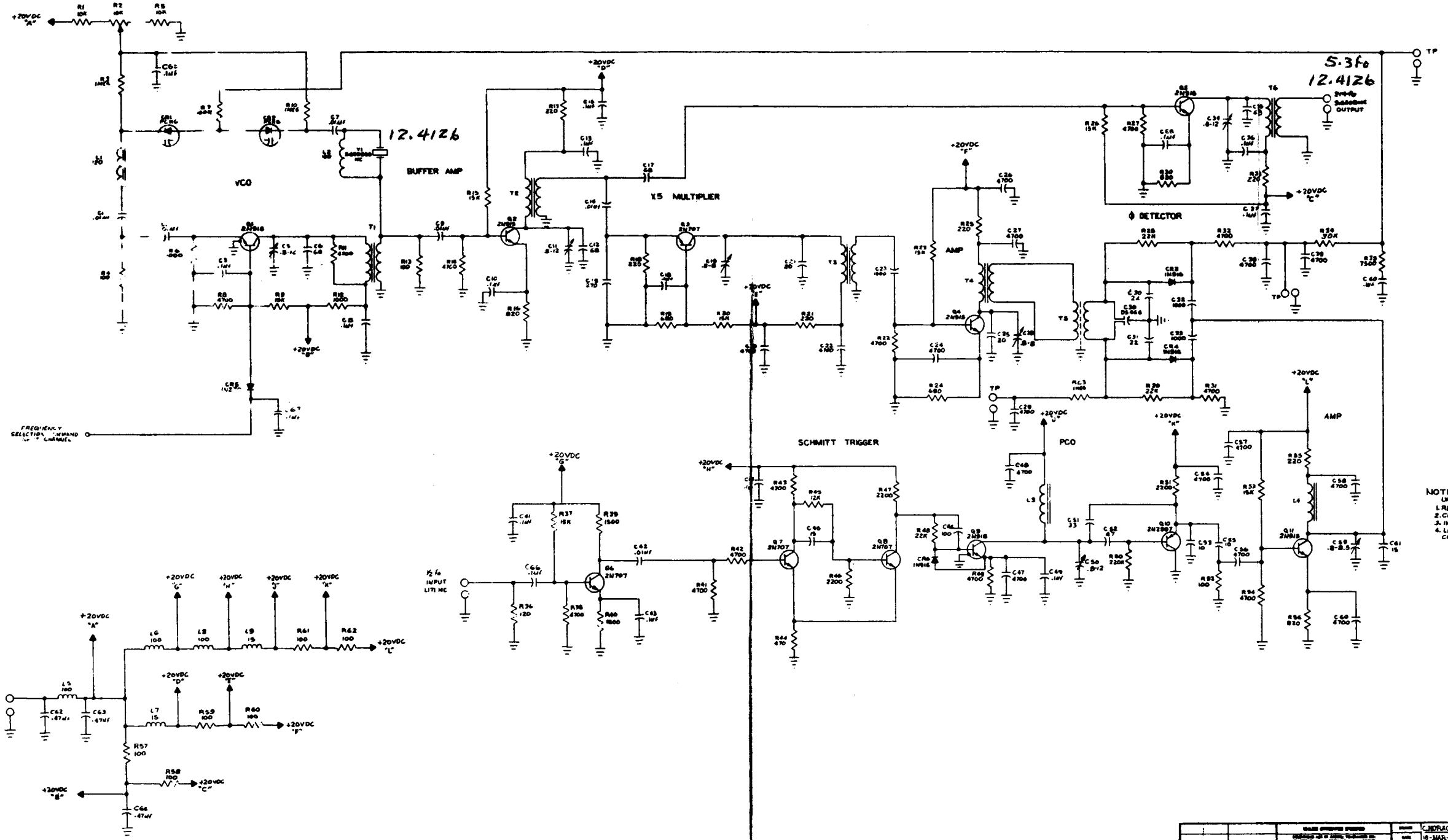
NOTES:
1. ALL RESISTORS ARE 1/4W 5%
2. ALL CAPACITORS IN pF UNLESS NOTED.
3. ALL INDUCTORS IN μh UNLESS NOTED
4. LAST REFERENCE DESIGNATIONS USED R66, C74, CR6, L15, T6, Q13
5. REFERENCE DESIGNATIONS NOT USED C40, C44, C54, C57, R23, R44

SCHEMATIC
X 76 MULTIPLIER LOOP

362093 | W0362

SCALE NONE

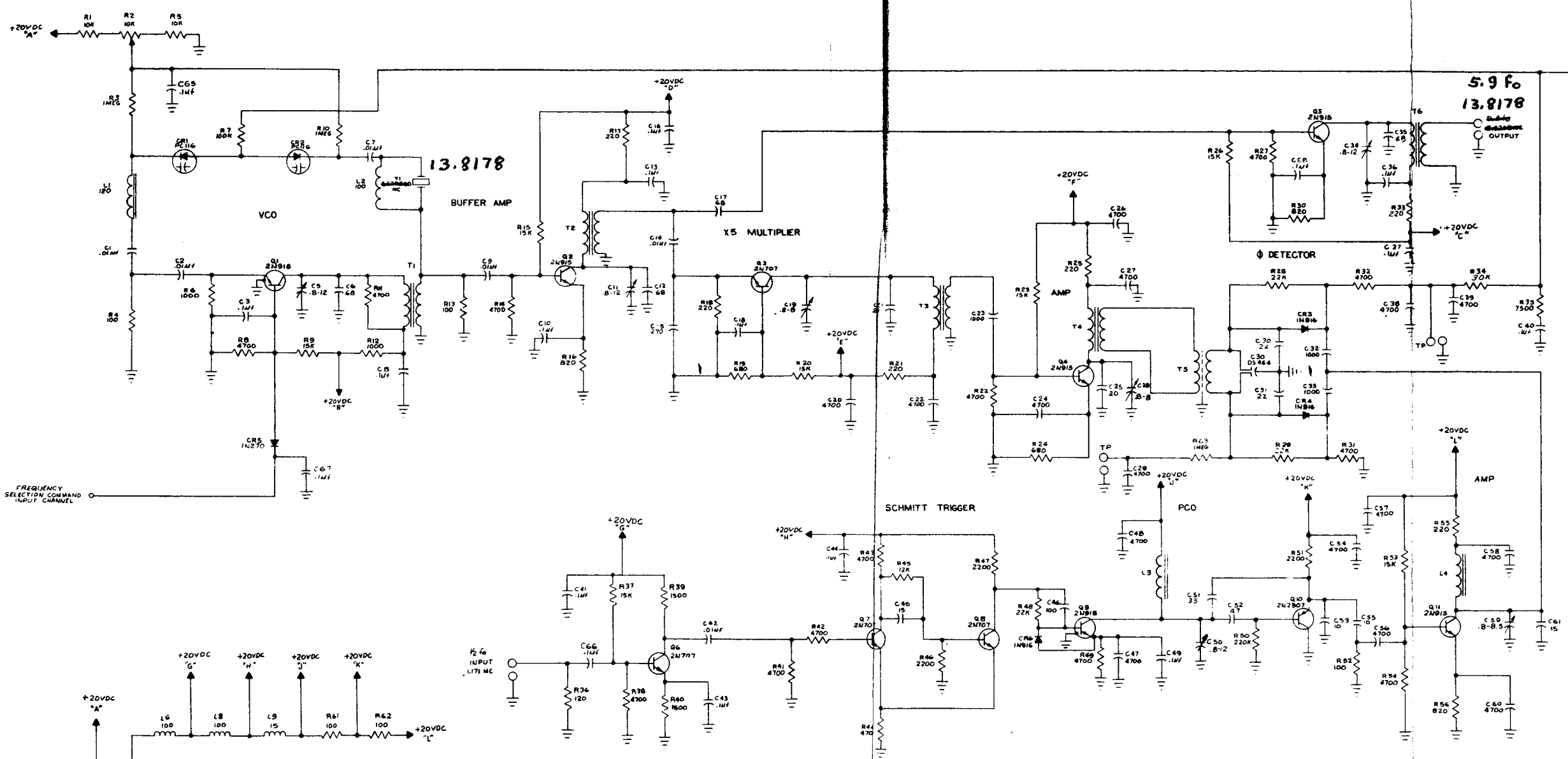
362162



NOTES:
UNLESS OTHERWISE NOTED
1. RESISTORS ARE IN OHMS 1/4W 5%
2. CAPACITORS ARE IN pf
3. INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATORS USED C66, CR6, L9, R62, T6, Φ11, Y1

A-06151

		C. MORRACE	SCHEMATIC	Sperry Gyroscope Co. Div. Sperry Rand Corp. Great Neck, N.Y.
		18-MAR-64	X10.6 MULTIPLIER LOOP AROD TRANSPONDER	
		K.S. 5-23-64		
D-362152 WO 362			NONE	SIZE E SD-362151



NOTES:
UNLESS OTHERWISE NOTED
1. RESISTORS ARE IN OHMS 1/4W 5%
2. CAPACITORS ARE IN pf
3. INDUCTORS ARE IN uh
4. LAST REFERENCE DESIGNATORS USED C66, CR6, L9, RG2, TG, Q11, Y1

		DRAWN	C. HORACE
		DATE	16-MAR-64
		ENGINEER	
		DATE	5-23-64
		APPROVED	
		DATE	
D-362153-1	WO 362		

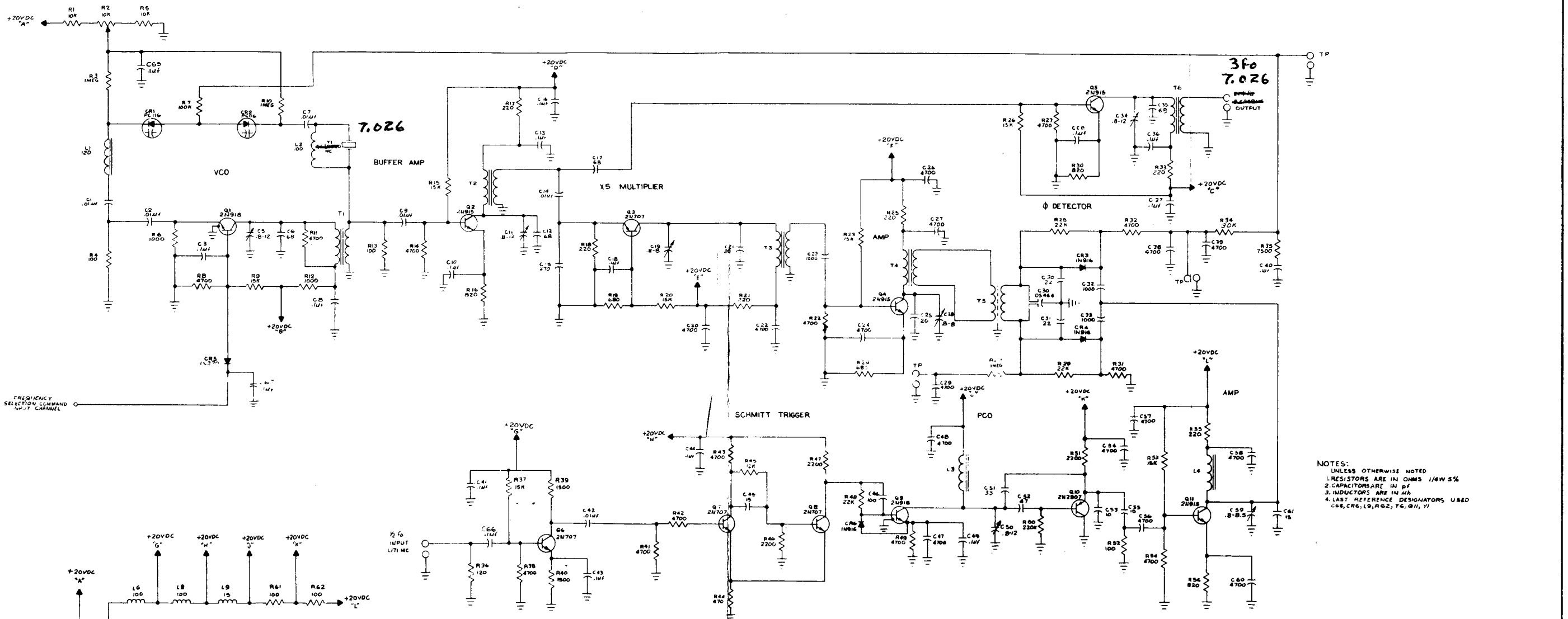
SCHEMATIC
X118 MULTIPLIER LOOP
AROD TRANSPONDER

NONE

SIZE E

SD-362153

4-06152



A-06142

			C. HOYACK	SCHEMATIC	Space Craft Inc. Huntsville, Ala.
			18-MAR-64	X6.0 MULTIPLIER LOOP	
			5-23-64	AROD TRANSPONDER	
0-362149	WO 362			NONE	SIZE E — SC-362148

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED

VCO

BUFFER AMP

X5 MULTIPLIER

Φ DETECTOR

AMP

SCHMITT TRIGGER

PCO

AMP

FREQUENCY SELECTION COMMAND INPUT CHANNEL

½ fo INPUT 1.171 MC

+20VDC INPUT

2.4 fo 5.6208 MC OUTPUT

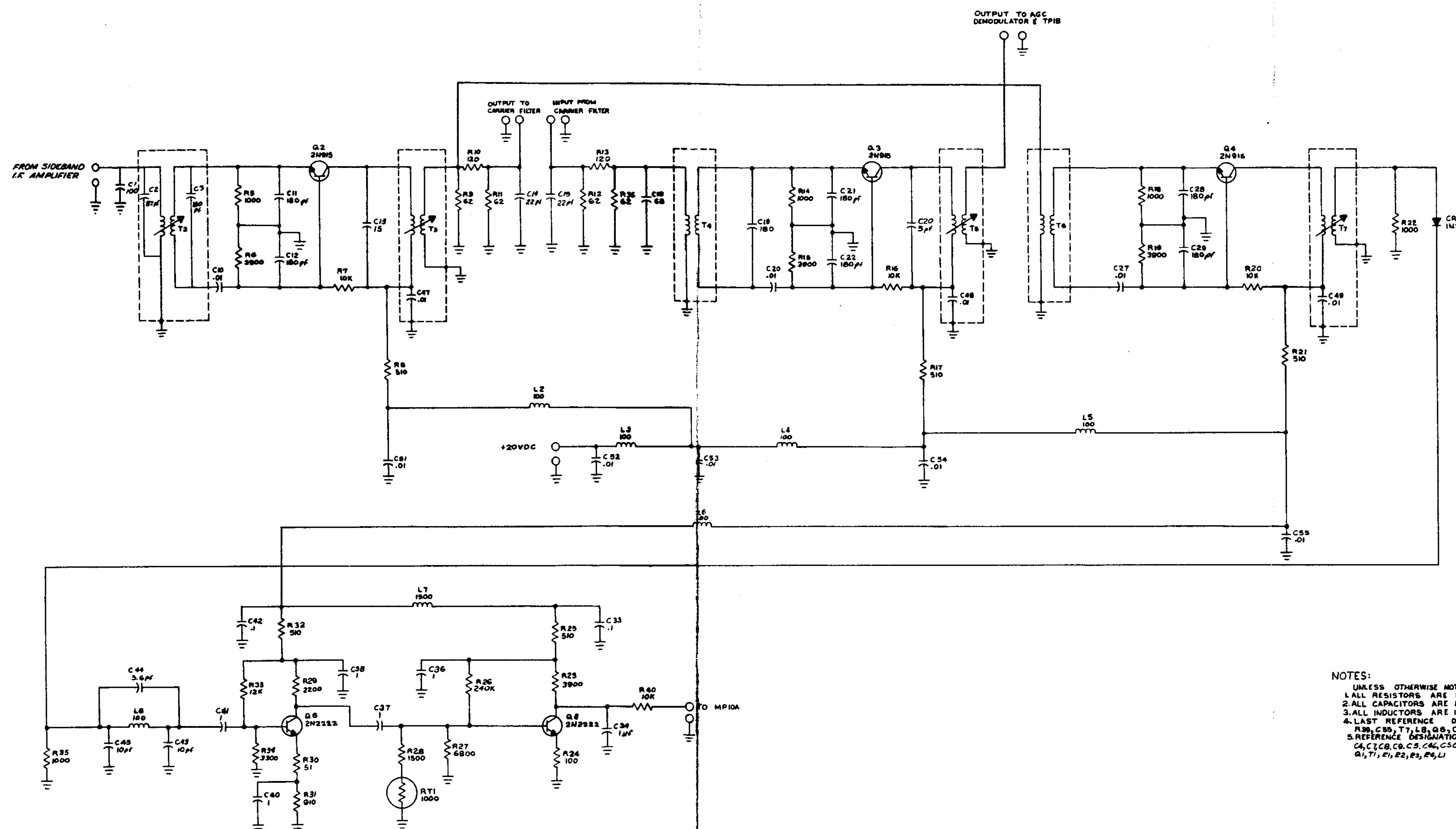
TP

NOTES:
UNLESS OTHERWISE NOTED
1. RESISTORS ARE IN OHMS 1/4W 5%
2. CAPACITORS ARE IN pf
3. INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATORS USED CR8, CR9, L9, R62, T6, Q11, Y1

A-06141

		UNLESS OTHERWISE SPECIFIED	DRAWN	C. HORN	SCHEMATIC
			DATE	18-MAR-64	X4.8 MULTIPLIER LOOP
		MATERIAL	CHECKED		AROD TRANSPONDER
		HEAT TREATMENT	DATE		
D-362147	WO 362	FINISH, PROTECTIVE FINISH	APPROVED		SIZE E
NEXT ASSY.	USED ON		DATE		SCI-362146
APPLICATION			NEXT ASSY		SHEET OF

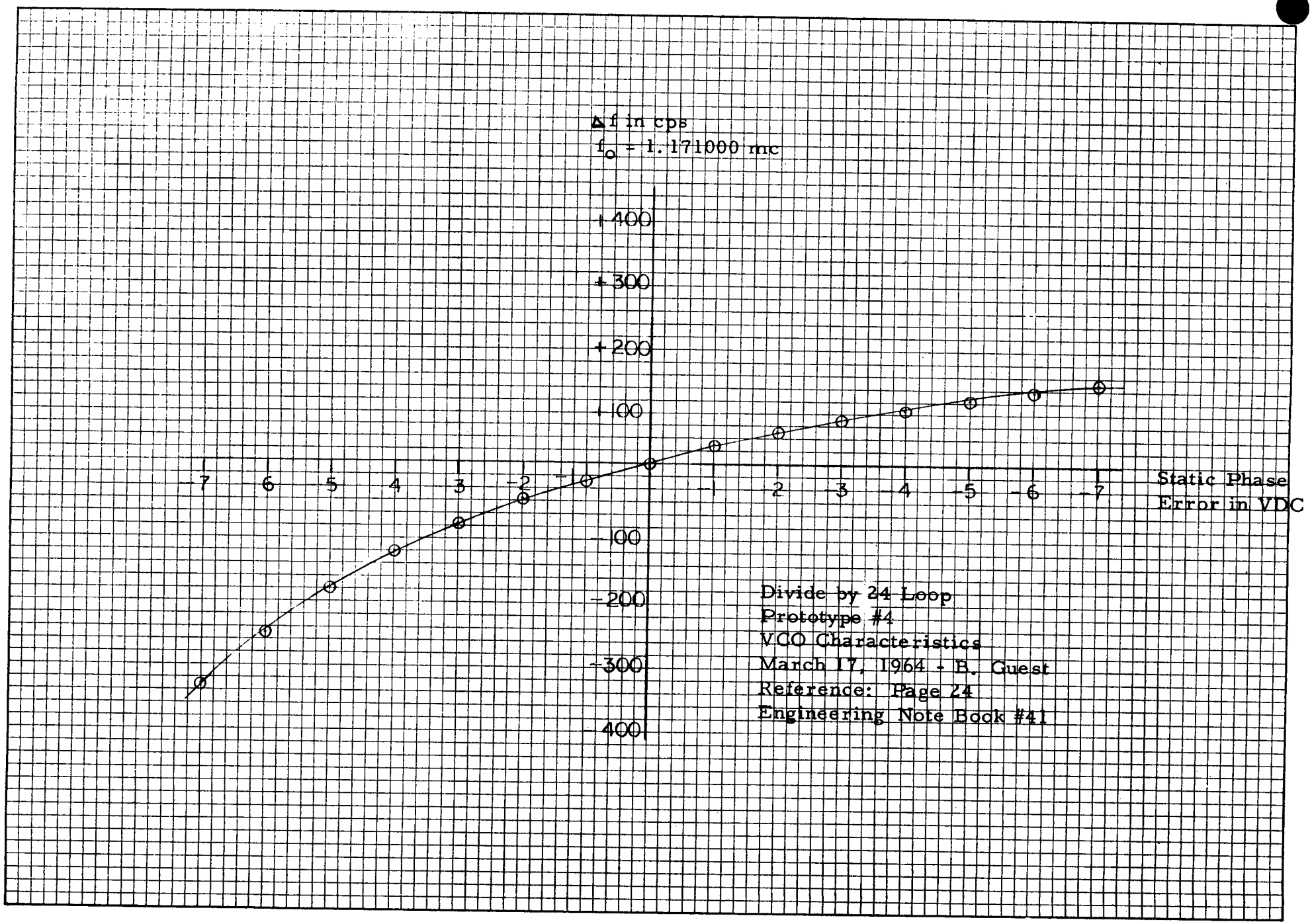
Space Craft Inc. Huntsville, Ala.

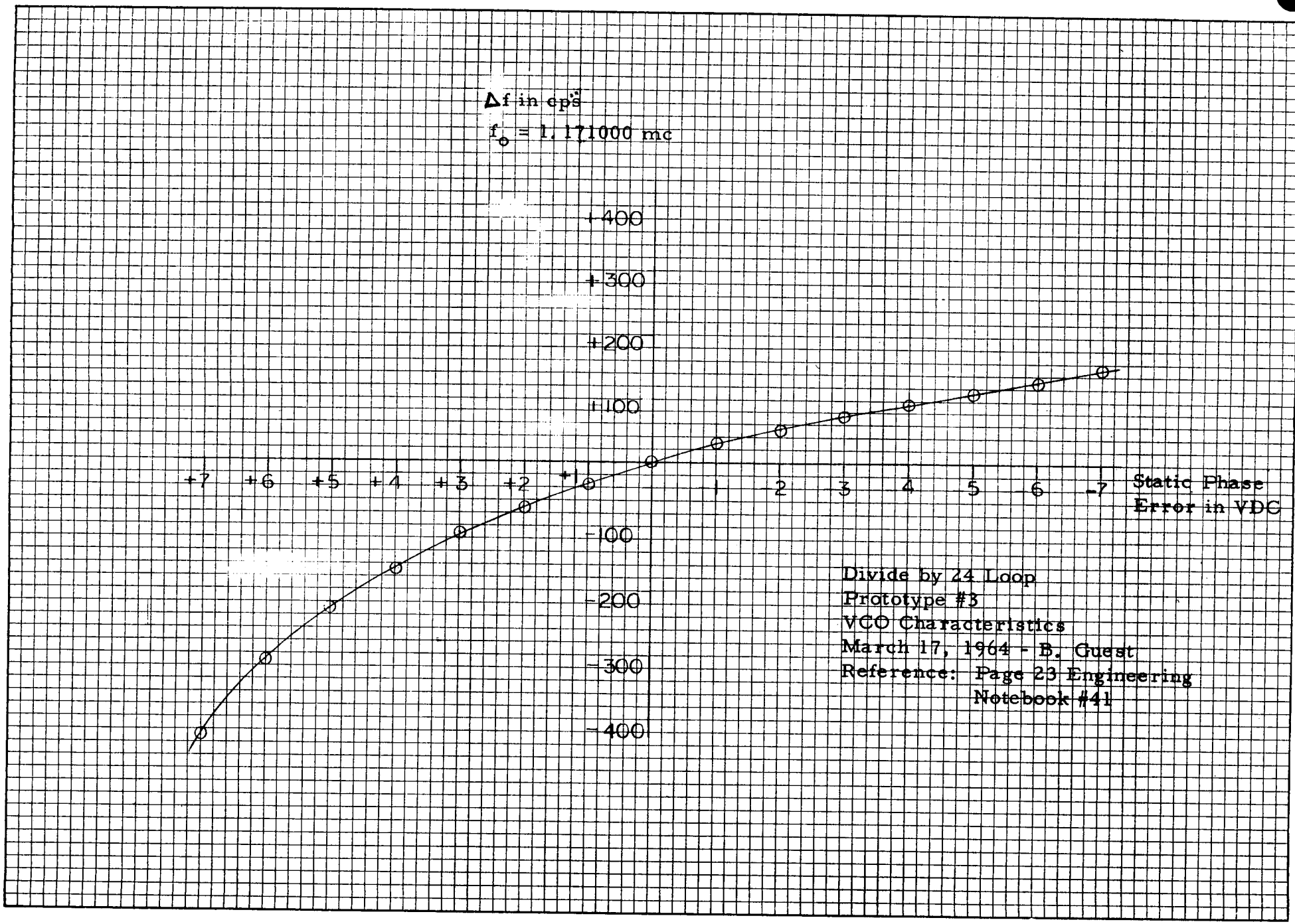


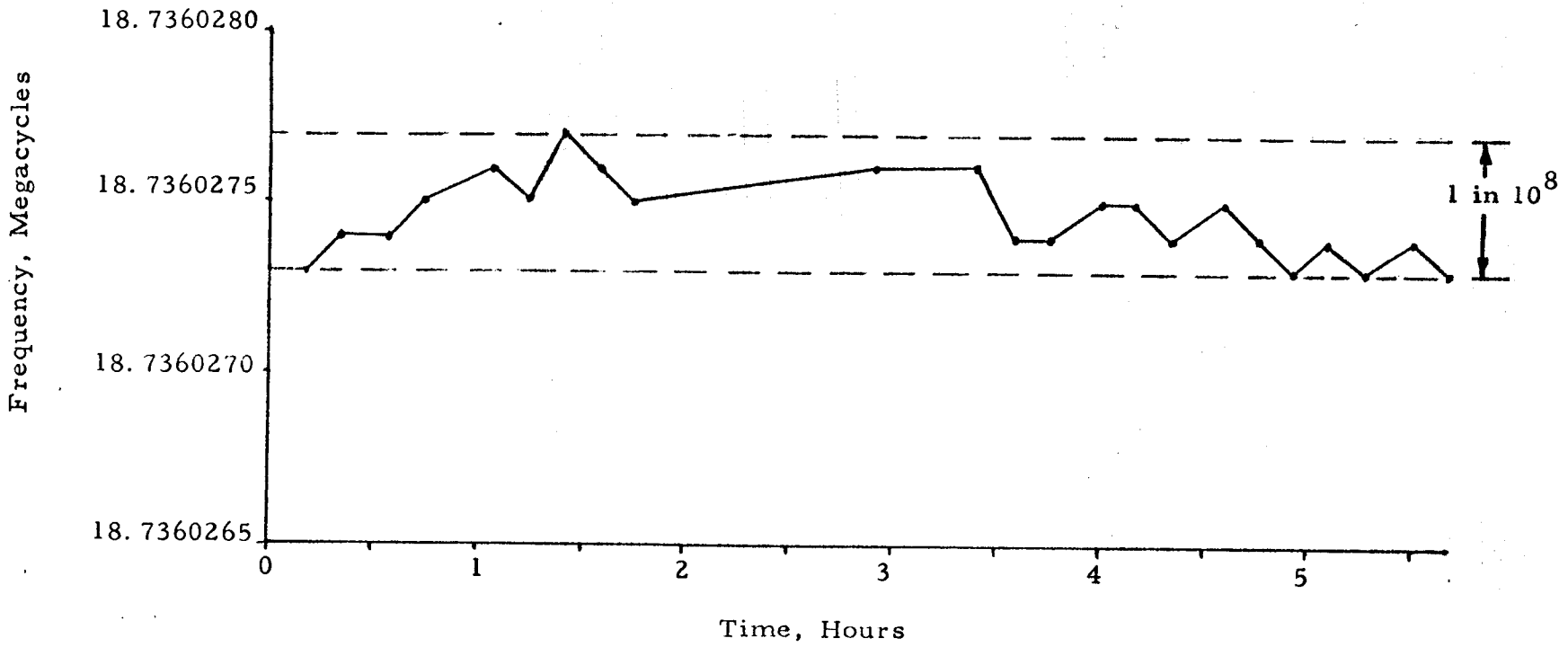
NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE IN OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN μf
3. ALL INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED:
R39, C55, T7, L8, Q6, CR1, RT1
5. REFERENCE DESIGNATIONS NOT-USED
C4, C7, C8, C9, C5, C46, C50, C23, C24, C25, C26, C31, C32, C35
Q1, T1, E1, E2, E3, E4, L1

A-02222

0362107	W0362	C. Horne 5-Feb-64	SCHEMATIC, CARRIER I.F. AMPLIFIER
Space Craft Inc. Huntsville, Ala.	J	SCI-362105	SCALE NONE


Δf in cps
f_o = 1.171000 mc
+400
+300
+200
+100
-100
-200
-300
-400
7
6
5
4
3
2
1
1
2
3
4
5
6
7
Static Phase Error in VDC
Divide by 24 Loop
Prototype #4
VCO Characteristics
March 17, 1964 - B. Guest
Reference: Page 24
Engineering Note Book #41

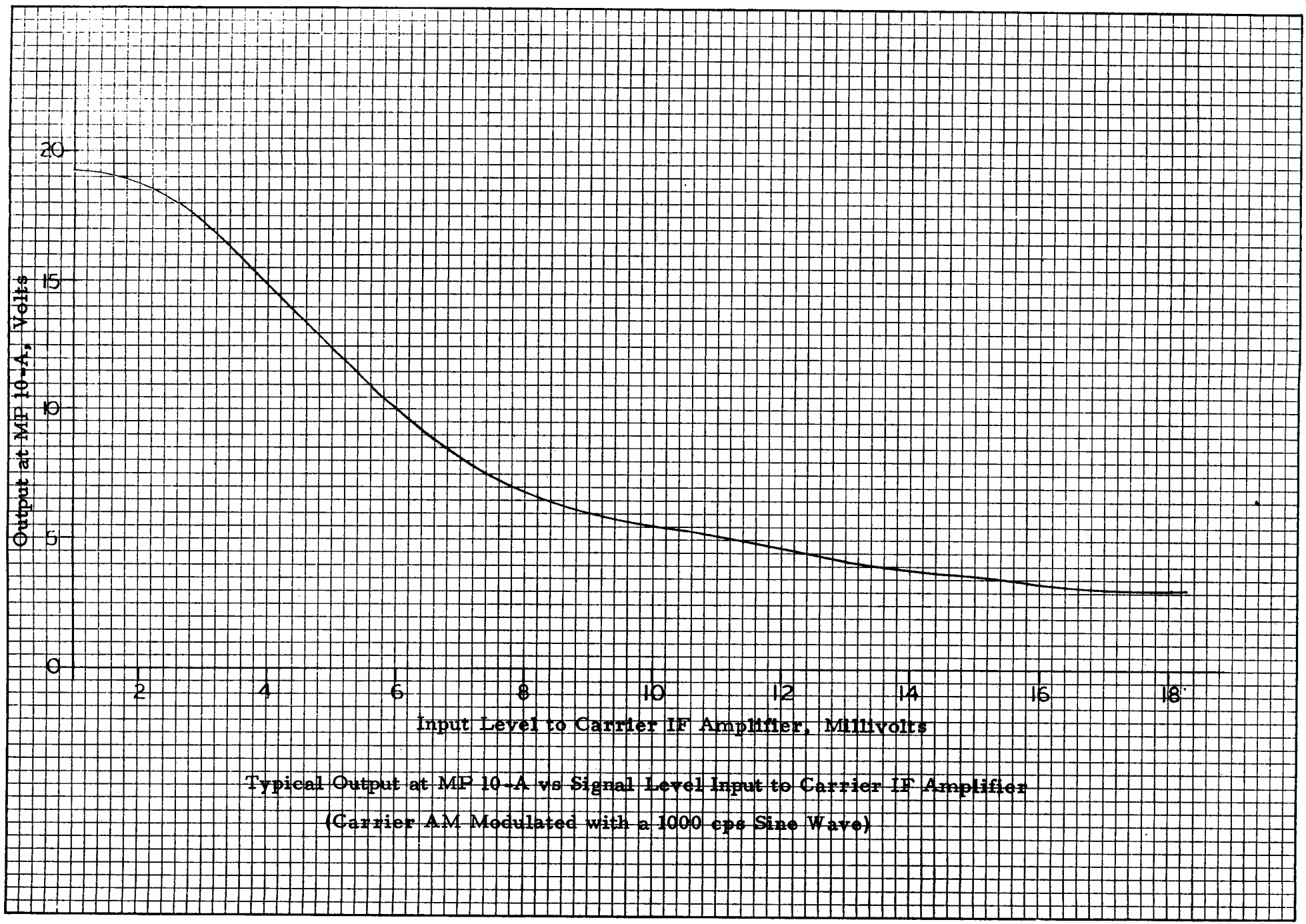

Δf in cps
f_o = 1. 171000 mc
+400
+300
+200
+100
-100
-200
-300
-400
+7
+6
+5
+4
+3
+2
+1
-1
-2
-3
-4
-5
-6
-7
Static Phase Error in VDC
Divide by 24 Loop
Prototype #3
VCO Characteristics
March 17, 1964 - B. Guest
Reference: Page 23 Engineering Notebook #41



18. 736 Megacycle Reference Oscillator

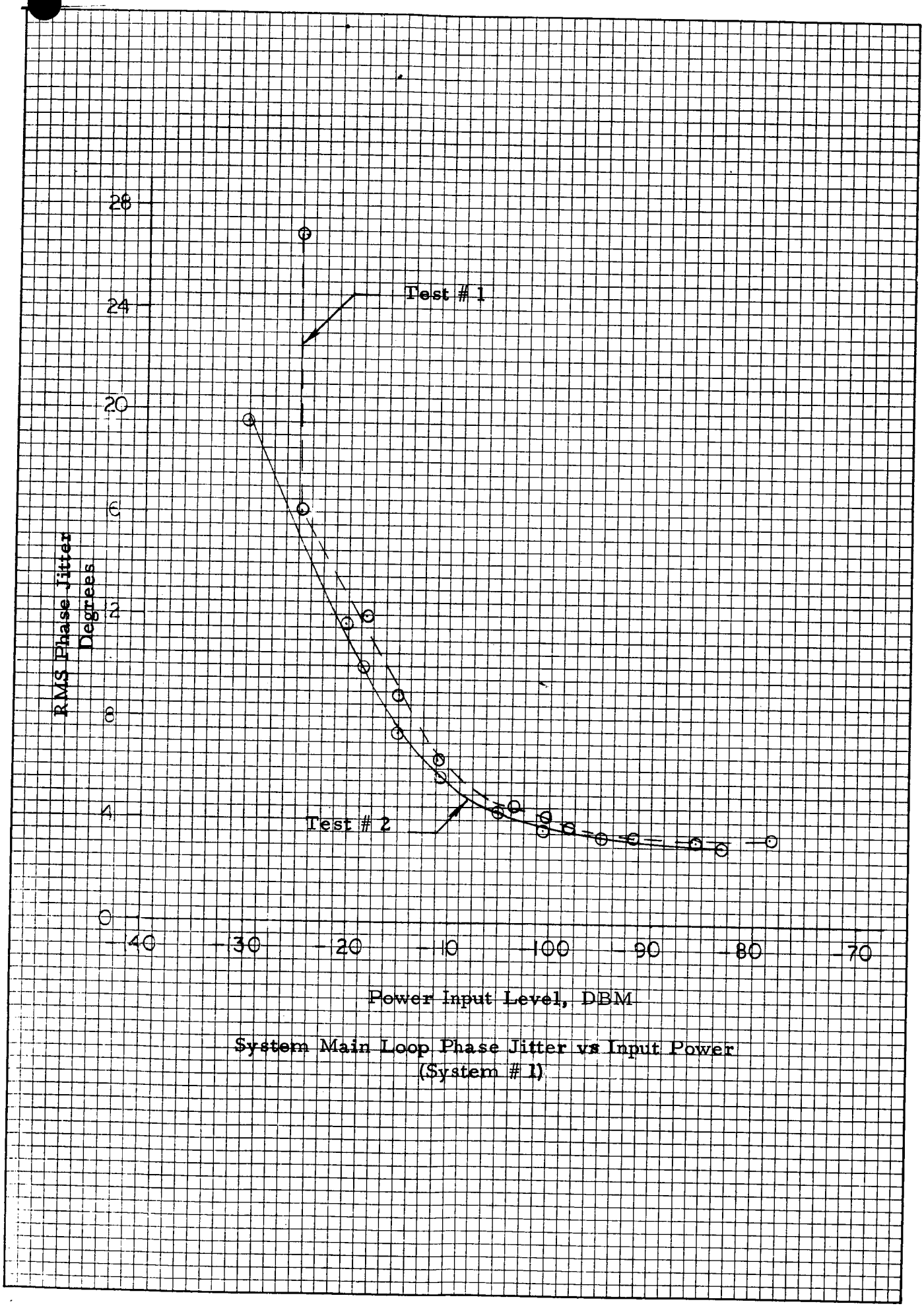
Frequency vs. Time for 5 2/3 Hours

Continuous Operation

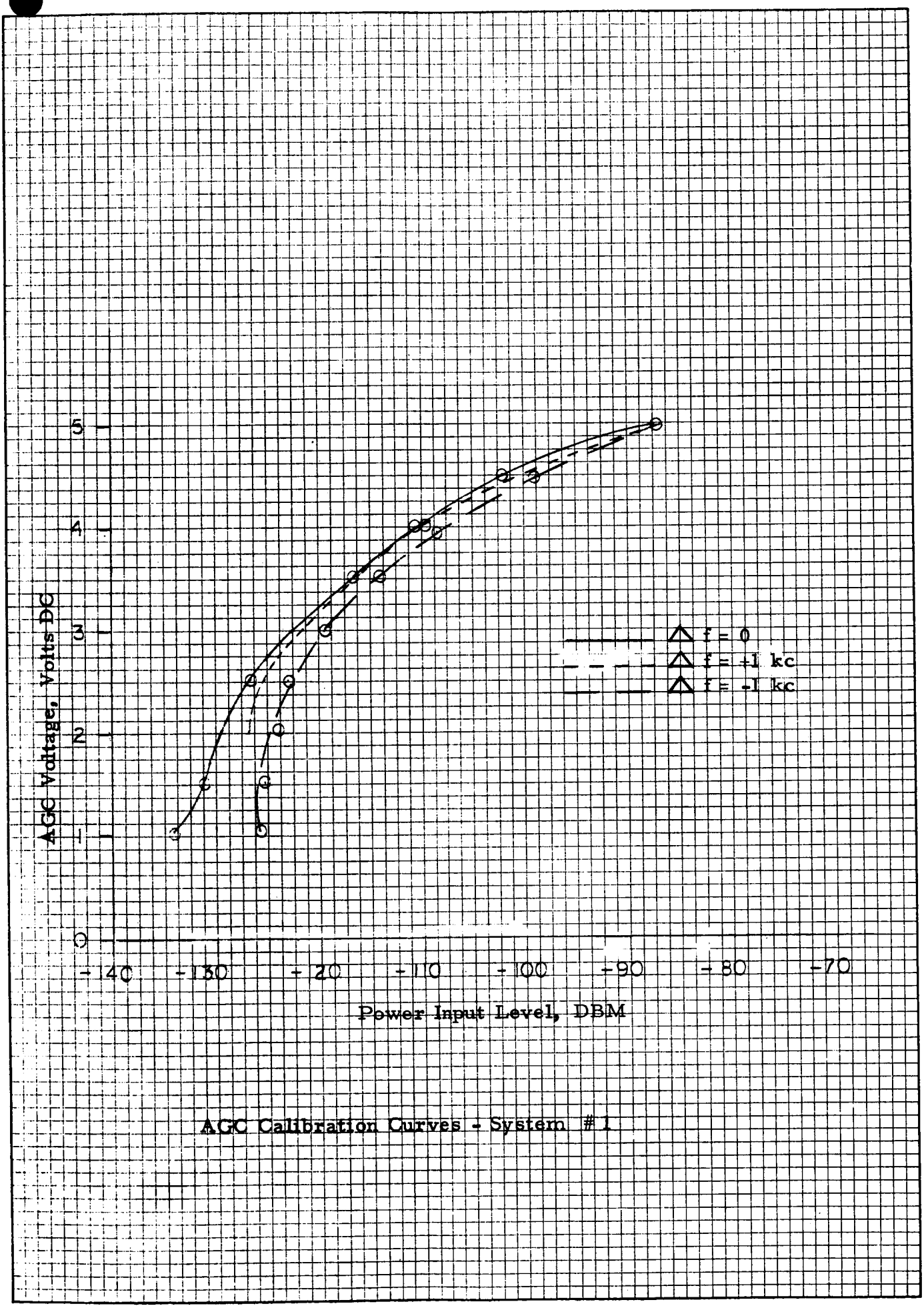


Typical Output at MP 10-A vs Signal Level Input to Carrier IF Amplifier

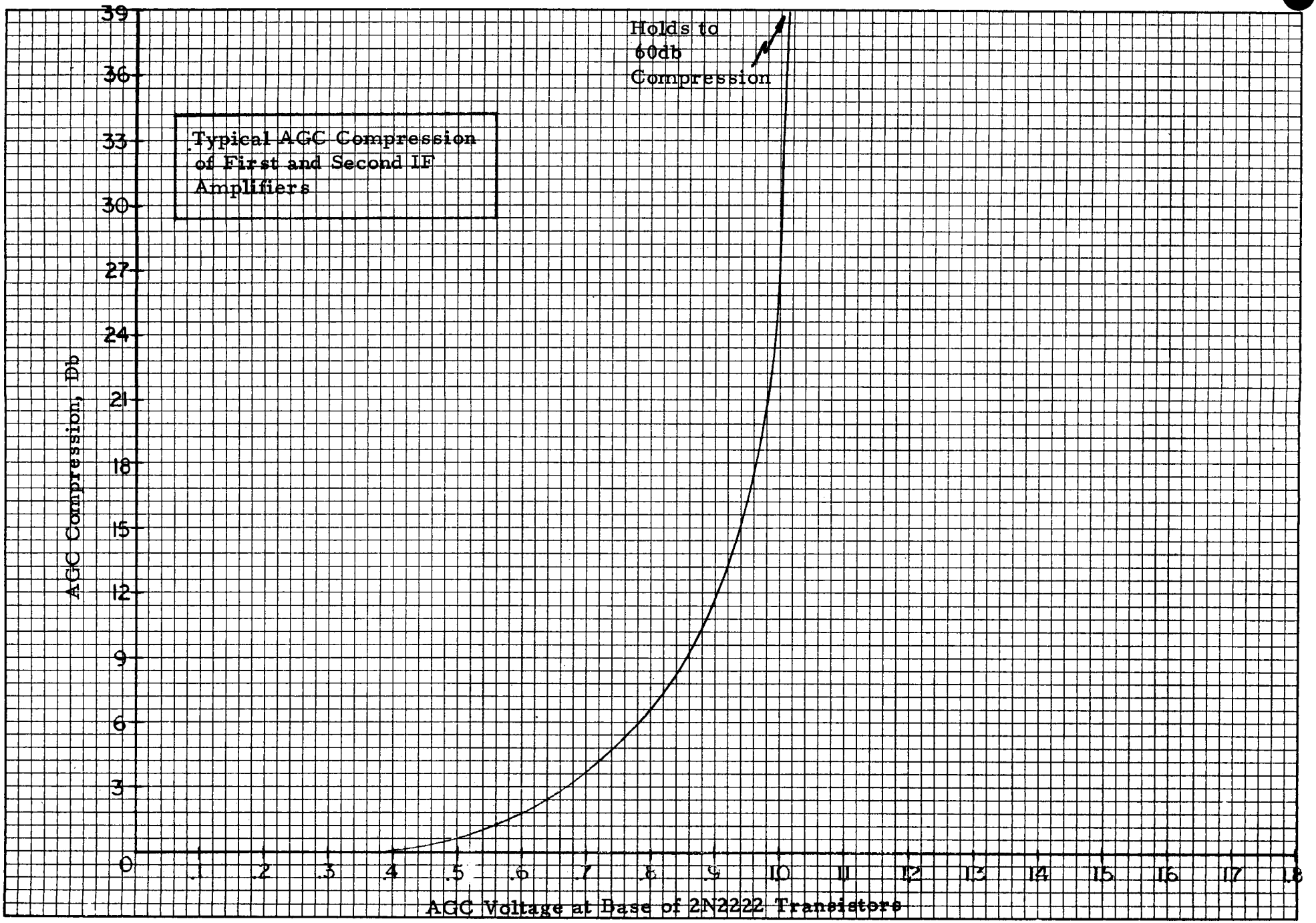
(Carrier AM Modulated with a 1000 cps Sine Wave)

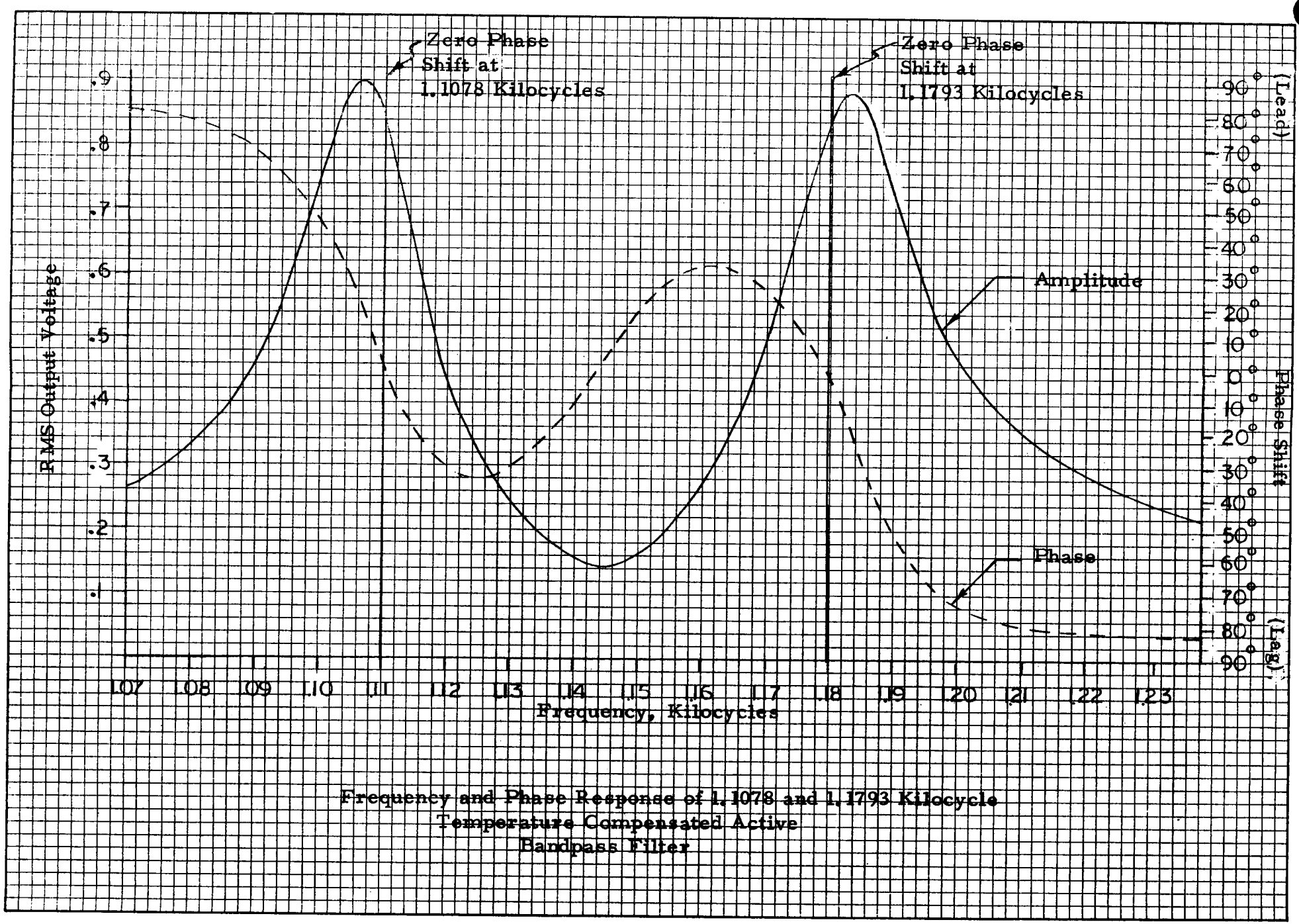


System Main Loop Phase Jitter vs Input Power
(System # 1)

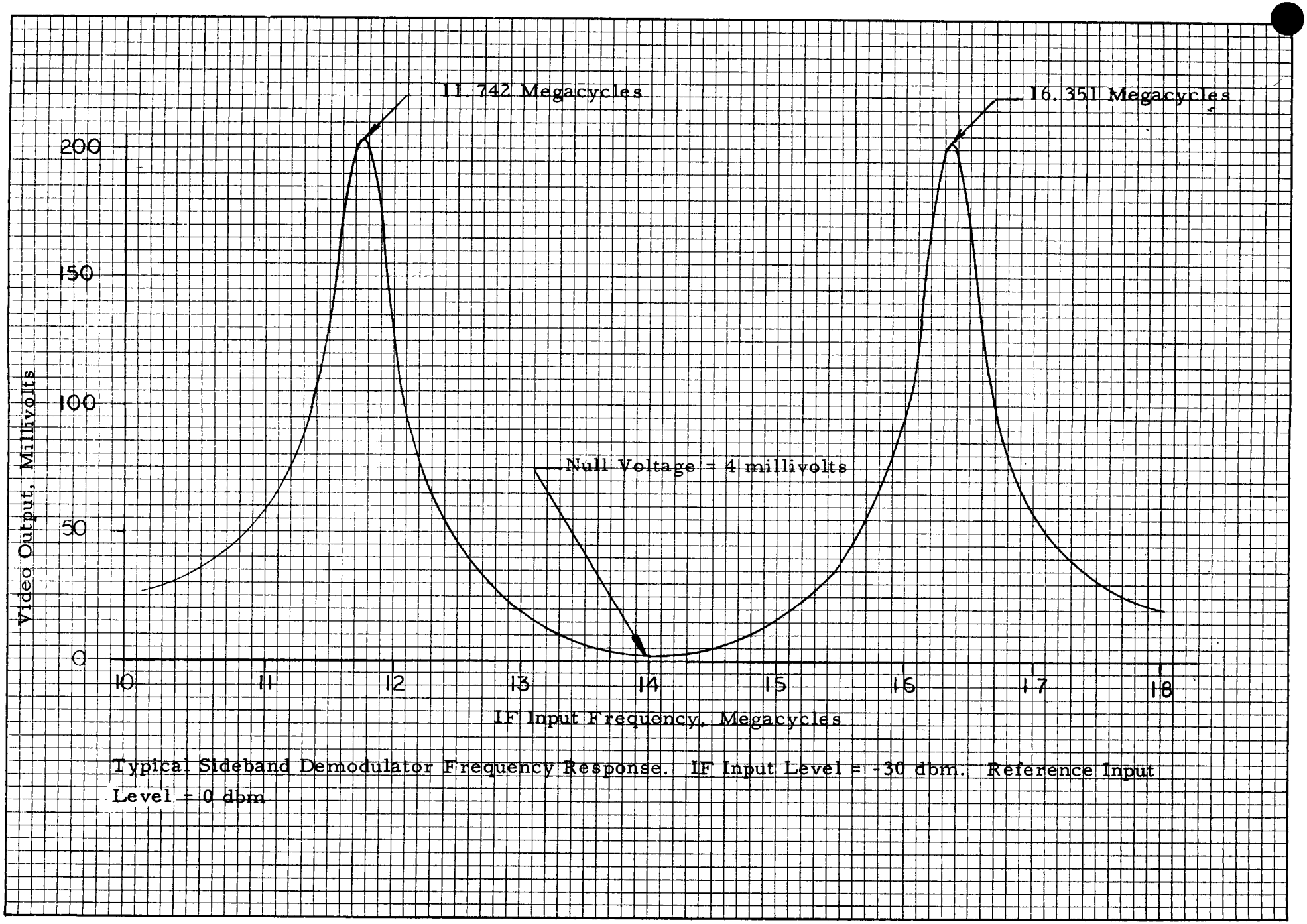


AGC Calibration Curves - System #1

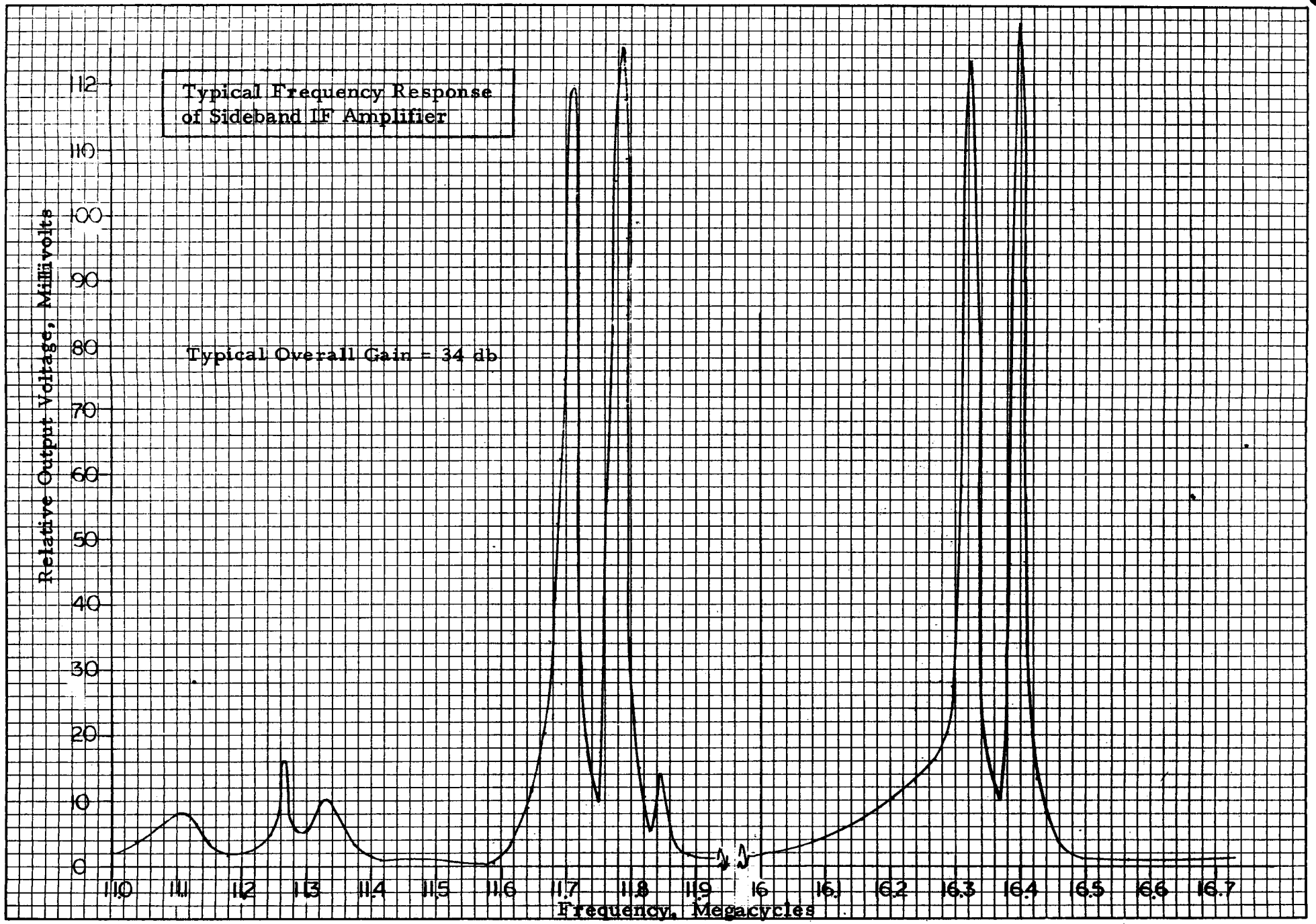

Typical AGC Compression of First and Second IF Amplifiers
Holds to 60db Compression
AGC Compression, Db
39
36
33
30
27
24
21
18
15
12
9
6
3
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
10
11
12
13
14
15
16
17
18
AGC Voltage at Base of 2N2222 Transistors

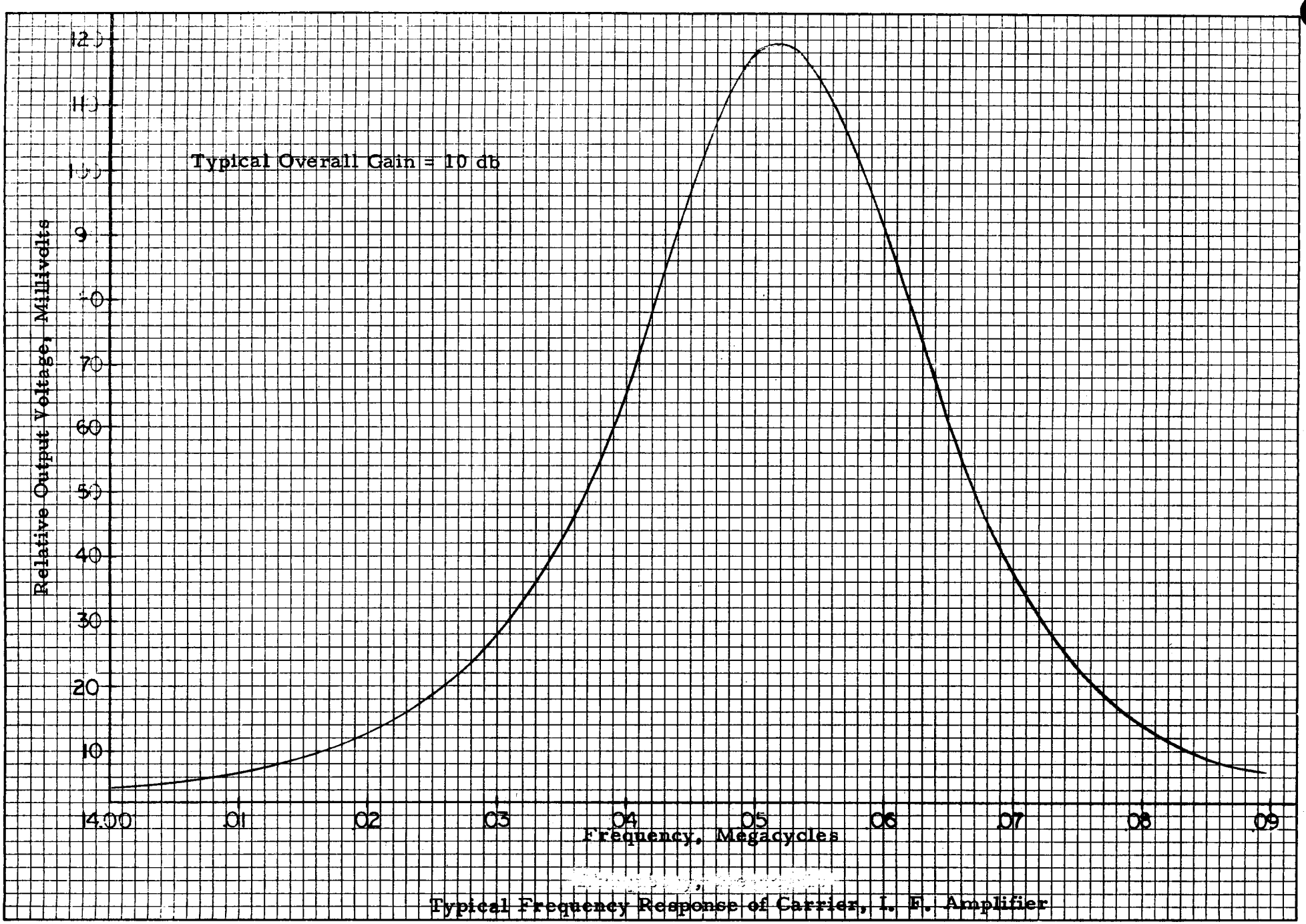


Frequency and Phase Response of 1.1078 and 1.1793 Kilocycle Temperature Compensated Active Bandpass Filter

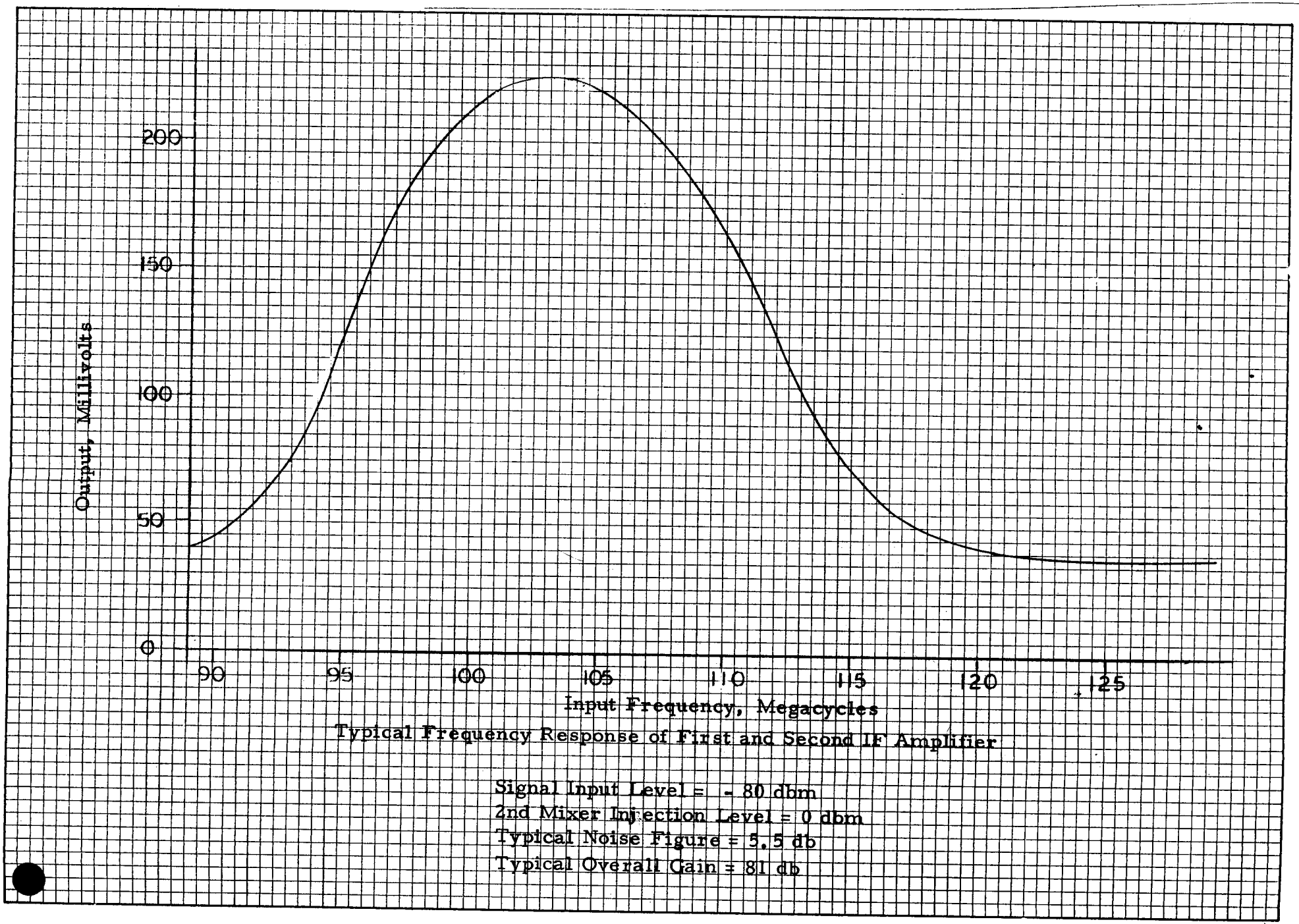


Typical Sideband Demodulator Frequency Response. IF Input Level = -30 dbm. Reference Input Level = 0 dbm


Typical Frequency Response
of Sideband IF Amplifier
Typical Overall Gain = 34 db
Relative Output Voltage, Millivolts
112
110
100
90
80
70
60
50
40
30
20
10
0
11.0
11.1
11.2
11.3
11.4
11.5
11.6
11.7
11.8
11.9
16
16.1
16.2
16.3
16.4
16.5
16.6
16.7
Frequency, Megacycles



Typical Frequency Response of Carrier, I. F. Amplifier



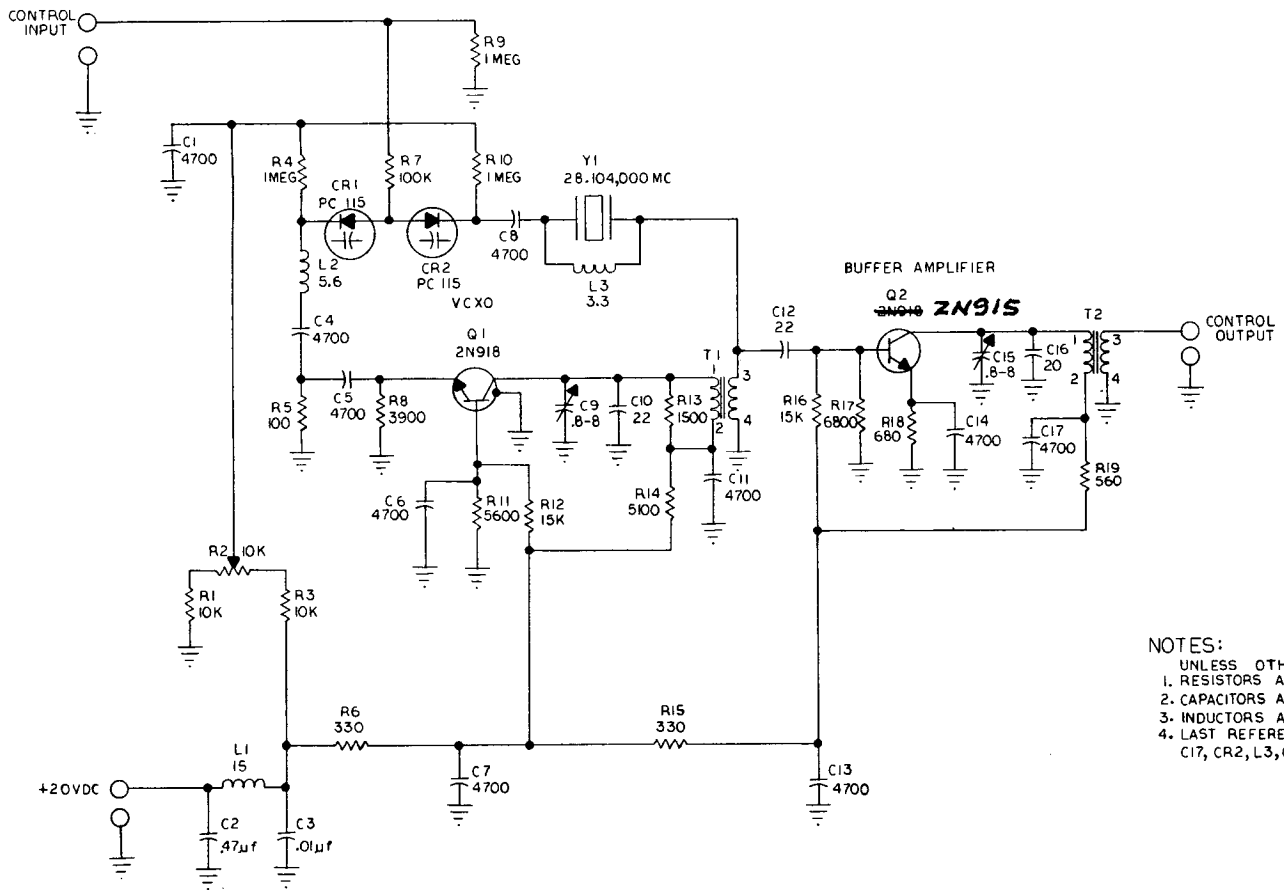
Typical Frequency Response of First and Second IF Amplifier

Signal Input Level = - 80 dbm
2nd Mixer Injection Level = 0 dbm
Typical Noise Figure = 5.5 db
Typical Overall Gain = 81 db

SECTION VI

TEST DATA

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL



NOTES:
UNLESS OTHERWISE NOTED
1. RESISTORS ARE IN OHMS 1/4W 5%
2. CAPACITORS ARE IN pf
3. INDUCTORS ARE IN μh
4. LAST REFERENCE DESIGNATIONS USED: C17, CR2, L3, Q2, R19, T2, Y1

A-02251

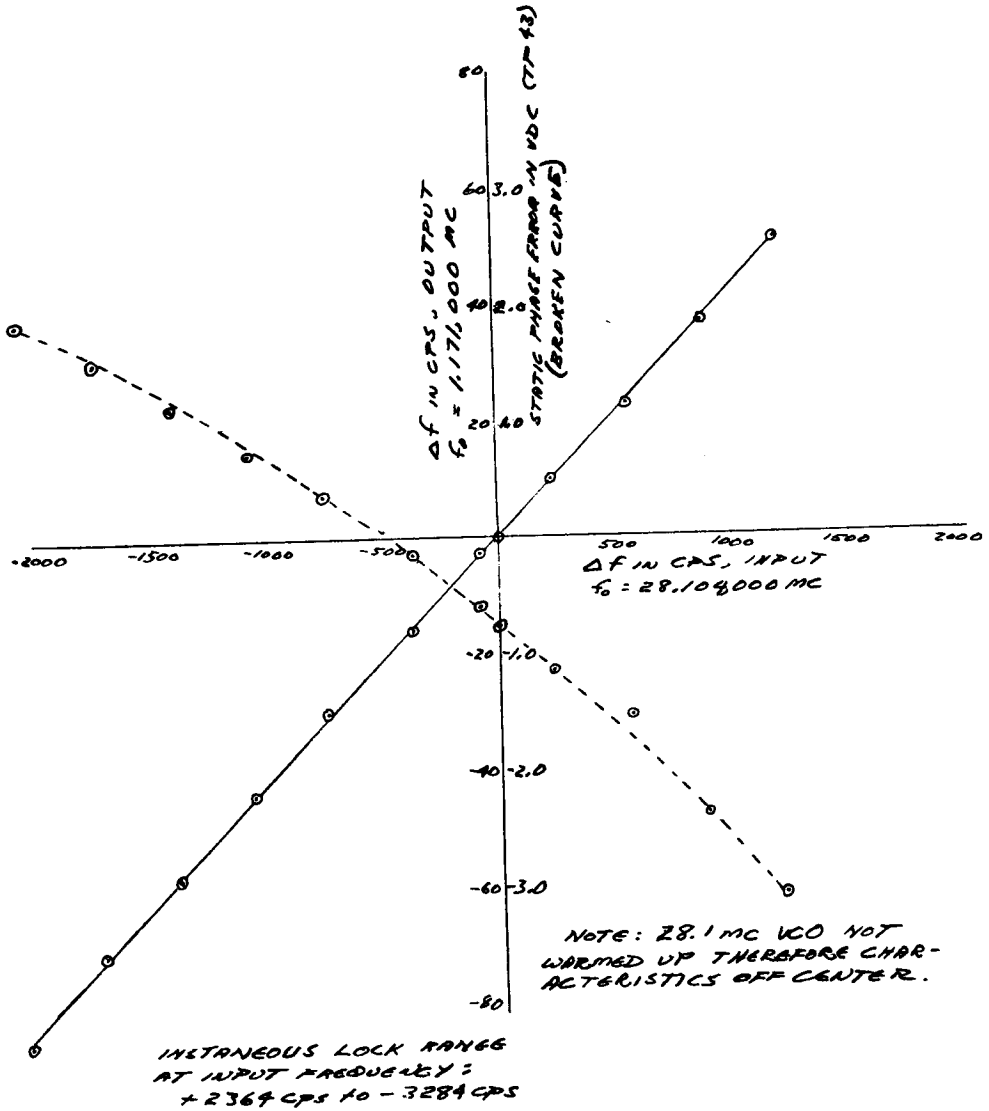
—3	—2	—1	ITEM NO.	DESCRIPTION	MIL. SPEC.	MFR'S. PT. NO. / DRAWING NO.	REMARKS / MFR'S CODE
NO. REQ'D. PER ASS'Y.			LIST OF MATERIALS				

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS, DECIMALS, ANGLES	DRAWN	C.HORACE	SCHEMATIC, 28.104 MC VCXO RECEIVER & TRANSMITTER
MATERIAL	DATE	7-APR-64	SPACE CRAFT Inc. Huntsville, Alabama
HEAT TREATMENT	CHECKED		
FINAL PROTECTIVE FINISH	DATE	9-8-69	
362182 / W0362 (NEXT ASSY. / USED ON)	APPROVED		SCALE NONE
APPLICATION	DATE		UNIT WT.
			DWG. SIZE C — SCI-362180 — REV.
			SHEET OF

SCI Form 810-015A

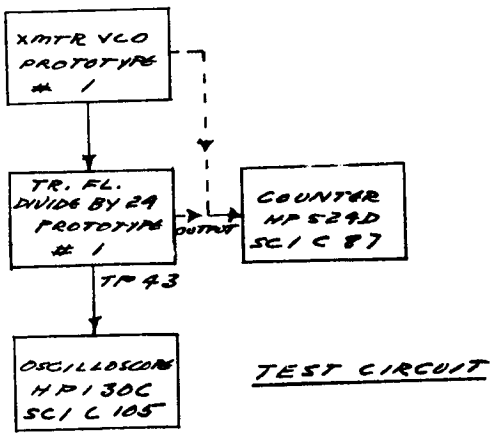
TRANSMITTER TRACKING FILTER
DIVIDE BY 24
CLOSED LOOP CHARACTERISTICS

VCO GAIN = 80 CPS/VOLT NOMINAL
PHASE DETECTOR GAIN = .0833 V/DEG NOM
$2B_L$ = 2000 CPS NOMINAL
FEBR 17, 69 TESTED BY: E. GOEST

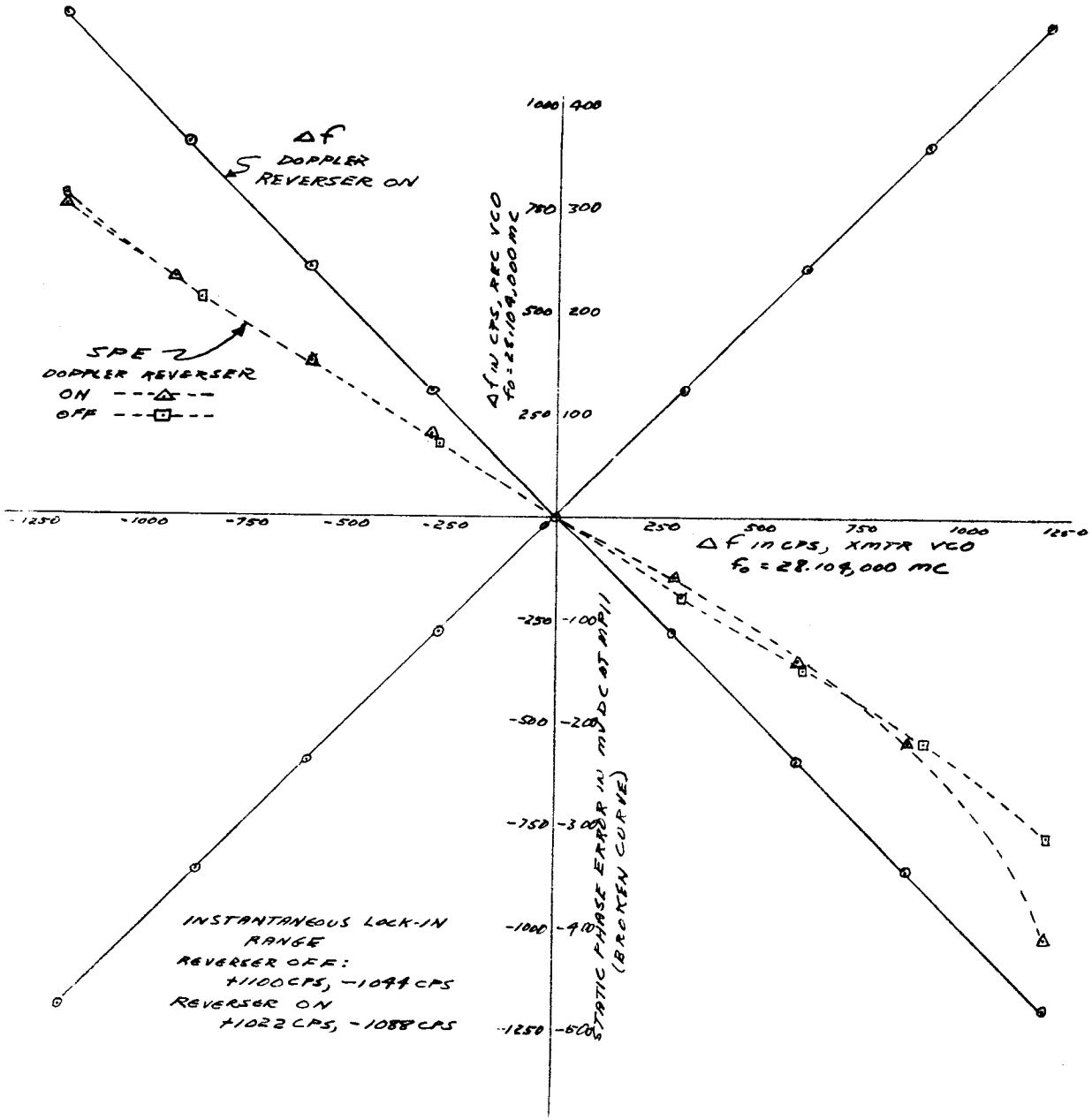


NOTE: 28.1 MC VCO NOT WARMED UP THEREFORE CHARACTERISTICS OFF CENTER.

INSTANEOUS LOCK RANGE AT INPUT FREQUENCY:
+2364 CPS TO -3284 CPS



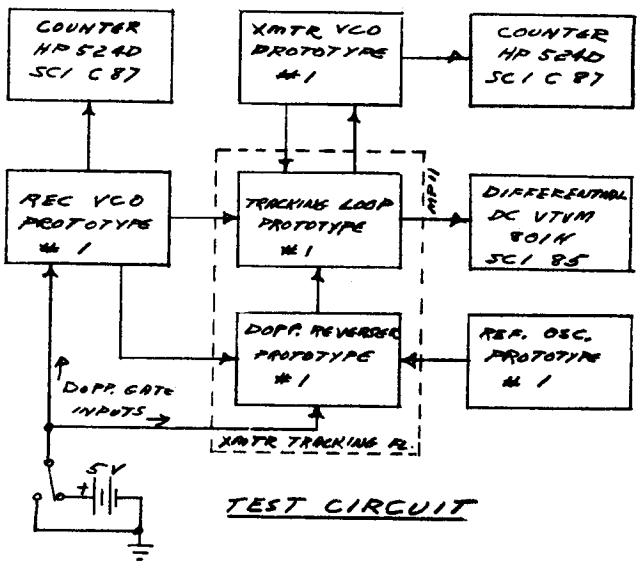
TEST CIRCUIT



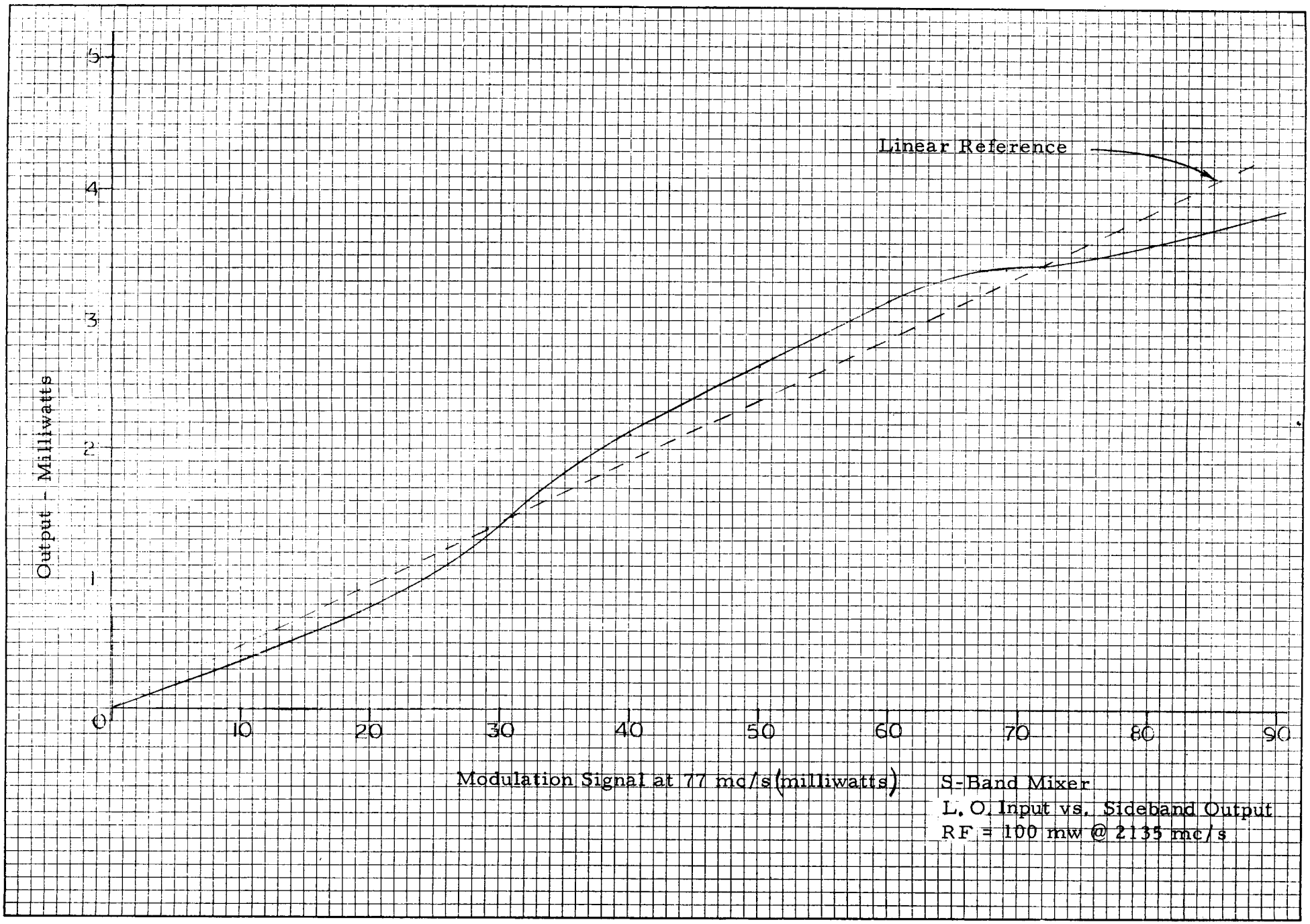
TRANSMITTER TRACKING FILTER
CLOSED LOOP CHARACTERISTICS
WITH
DOPPLER REVERSER
OFF AND ON

XMTR VCO GAIN = 300 CPS/VOLT NOMINAL
PHASE DETECTOR GAIN = .0833 V/DEG NOM
$2B_L$ = 1200 CPS NOM., CALCULATED

FEBR 24, 1964 TESTED BY: B. GUEST



TEST CIRCUIT


Linear Reference
Output - Milliwatts
0
1
2
3
4
5
10
20
30
40
50
60
70
80
90
Modulation Signal at 77 mc/s (milliwatts)
S-Band Mixer
L. O. Input vs. Sideband Output
RF = 100 mw @ 2135 mc/s

DATA SHEET

AROD TRANSPONDER

Circuit Board 2.342 RANGE TONE Loop S/N PROTO TYPE

Date JAN 21, 1964 Test By B Guest

Loop Characteristics

VCO Frequency: -5 VDC 2.342.263 mc/sec

0 VDC 2.342.009 mc/sec

+5 VDC 2.342.660 mc/sec

VCO Gain (±1VDC) 139 cps/volt

Ø Det. "S" Curve 1 VOLT NOMINAL * volts peak

Ø Det. Gain (Calculated) .0167 volts. Deg.
0 MV TO -5 VDC

Ø Det. Balance 120 MV (.4%) AT +10 VDC MVDC

Open Loop Gain ($360K_VK_DK_M$) 6.2 sec^{-1}

Noise Bandwidth ($2B_L$) 18.6 cps

Time Constants T_1 221 msec

T_2 15 msec

Input-Output Characteristics

Input Frequency 2.342 mc/sec

Input Power ____ dbm

Output Frequency 2.342 mc/sec

Output Power (50 ohm load) +20 dbm

* SEE ATTACHED OUTPUT CURVE

DATA SHEET

AROD TRANSPONDER

Circuit Board 2.342 mc LOOP S/N PROTOTYPE #2

Date 3-26-64 Test By B GUEST

Loop Characteristics

VCO Frequency:	-5 VDC	2.341043	mc/sec
	0 VDC	2.341997	mc/sec
	+5 VDC	2.342888	mc/sec
VCO Gain (±1VDC)		175	cps/volt
Ø Det. "S" Curve		1 NOMINAL *	volts peak
Ø Det. Gain (Calculated)		.0167	volts/Deg.
Ø Det. Balance		± 20	MVDC
Open Loop Gain ($360K_VK_DK_M$)		1055	sec^{-1}
Noise Bandwidth ($2B_L$)		100	cps
Time Constants	T_1	105	msec
	T_2	15	msec

Input-Output Characteristics

Input Frequency	2.342 mc	mc/sec
Input Power		dbm
Output Frequency	2.342 mc	mc/sec
Output Power (50 ohm load)	+11.7	dbm

* SEE ATTACHED OUTPUT CURVE

DATA SHEET

AROD TRANSPONDER

Circuit Board 2.268MC RANGE TONE LP S/N PROTOTYPE

Date 1-18-64 Test By B Guest

Loop Characteristics

VCO Frequency:	-5 VDC	2.268202	mc/sec
	0 VDC	2.269811	mc/sec
	+5 VDC	2.269730	mc/sec
VCO Gain (±1VDC)		112	cps/volt
Ø Det. "S" Curve		1.5	volts peak
Ø Det. Gain (Calculated)		.025	volts/Deg.
Ø Det. Balance		20 MAX	MVDC
Open Loop Gain ($360K_VK_DK_M$)		1010 ST. SIG 197 THRESH.	sec^{-1}
Noise Bandwidth ($2B_L$)		157.6 ST. SIGNAL 100 THRESH.	cps
Time Constants	T_1	22	msec
	T_2	15	msec

Input-Output Characteristics

Input Frequency	2.268	mc/sec
Input Power	-30 to +20	dbm
Output Frequency	2.268	mc/sec
Output Power (50 ohm load)	+11.0	dbm

INPUT LIMITING: -30 TO +20 DBM

DATA SHEET

AROD TRANSPONDER

Circuit Board 2.268 PL Loop S/N PROTOTYPE #2

Date MAR 19, 1964 Test By B GUEST

Loop Characteristics

VCO Frequency:	-5 VDC	2.26793	mc/sec
	0 VDC	2.268804	mc/sec
	+5 VDC	2.269648	mc/sec
VCO Gain (±1VDC)		164	cps/volt
Ø Det. "S" Curve		1.5	volts peak
Ø Det. Gain (Calculated)		.075	volts/Deg.
Ø Det. Balance		± 50	MVDC
Open Loop Gain ($360K_VK_DK_M$)		1475	sec^{-}
Noise Bandwidth ($2B_L$)		100	cps
Time Constants	T_1	16.45	msec
	T_2	15	msec

Input-Output Characteristics

Input Frequency	2.268812	mc/sec
Input Power	-20 TO +10	dbm
Output Frequency	2.268812	mc/sec
Output Power (50 ohm load)	± 1.2	dbm

VII. CONCLUSIONS

The design approach proposed by SCI and approved by NASA at the beginning of the AROD Transponder development program has proven extremely successful. The frequency scheme and frequency synthesizing techniques have worked as well as, and in many cases, better than anticipated. The method for obtaining fast acquisition by presetting the main VCXO's in the frequency domain has been shown to be feasible and practical. A somewhat new and different packaging technique for the type of circuits involved has demonstrated the feasibility and numerous advantages in terms of RFI shielding, adaptability to relatively low-cost and easily reproduced production assembly, and maximum versatility for incorporation of future changes with a minimum of redesign effort.

The various PCO, VCXO, and phase detector circuits have worked well over a wide range of operating frequencies from 1.171 mc to 170.26 mc. The 75 - 85 mc phasing-type single sideband generator has generally worked well except for the carrier and unwanted sideband suppression being only about 30 db as opposed to a desired suppression of 45 db.

A major problem peculiar to the single sideband plus carrier type of output spectrum was found to exist in the high-level S-band mixer.

In particular, sufficient linearity could not be obtained to provide reasonably low distortion products at the mixer output at the required power levels. The stripline mixer used in these transponders was purchased from Sanders Associates and represents near state-of-the-art design. A detailed analysis of the problem by Sanders indicated that no significant improvement in performance could be achieved with conventional rather than stripline construction techniques.

Thus, it appears that the problem of maintaining low spurious outputs is most severe with this type of output spectrum. Major breakthroughs in design of both the phasing-type sideband generator and the S-band high-level mixer would be necessary to achieve the desired 45 db suppression of spurious output signals while still maintaining the desired low (1 to 2 degrees) phase error on the fine range tone due to differential Doppler shifts.

DATA SHEET

AROD TRANSPONDER

Circuit Board DIVIDE By 24 Loop S/N PROTOTYPE

Date JAN 20, 1964 Test By B Guest

Loop Characteristics

VCO Frequency:	-5 VDC	1.171092	mc/sec
	0 VDC	1.171003	mc/sec
	+5 VDC	1.170859	mc/sec
VCO Gain (±1VDC)		23.3	cps/volt
Ø Det. "S" Curve		.5	volts peak
Ø Det. Gain (Calculated)		.0833	volts/Deg.
Ø Det. Balance		~5 (MAX)	MVDC
Open Loop Gain ($360K_VK_DK_M$)		16,800	sec^{-1}
Noise Bandwidth ($2B_L$)		2120	cps
Time Constants	τ_1	~~8.7~~ 4.2	msec
	τ_2	.78	msec

Input-Output Characteristics

Input Frequency	28.104	mc/sec
Input Power	0	dbm
Output Frequency	1.171	mc/sec
Output Power (50 ohm load)	0	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board DIVIDE By 24 S/N PROTOTYPE #3

Date MAR 17, 1964 Test By B. GUEST

Loop Characteristics

VCO Frequency: -5 VDC	1.121116	mc/sec
0 VDC	1.121002	mc/sec
+5 VDC	1.120764	mc/sec
VCO Gain (±1VDC)	238	cps/volt
Ø Det. "S" Curve	2.5	volts peak
Ø Det. Gain (Calculated)	.125	volts/Deg.
Ø Det. Balance	I 200	MVDC
Open Loop Gain ($360K_VK_DK_M$)	30,200	sec^{-1}
Noise Bandwidth ($2B_L$)	2200	cps
Time Constants T_1	8.5	msec
T_2	.75	msec

Input-Output Characteristics

Input Frequency	28.104	mc/sec
Input Power	+ 10	dbm
Output Frequency	1.121	mc/sec
Output Power (~~50~~ 15 ohm load)	+ 1.72 mW	~~dbm~~

DATA SHEET

AROD TRANSPONDER

Circuit Board DIVIDE By 24 S/N PROTOTYPE #4

Date MARCH 19, 1964 Test By C. FAUST

Loop Characteristics

VCO Frequency:	-5 VDC	1.171102	mc/sec
	0 VDC	1.171002	mc/sec
	+5 VDC	1.170803	mc/sec
VCO Gain (±1VDC)		[illegible]	cps/volt
Ø Det. "S" Curve		9.5	volts peak
Ø Det. Gain (Calculated)		.154	volts/Deg.
Ø Det. Balance		± .200	MVDC
Open Loop Gain ($360K_VK_DK_M$)		38,800	sec^{-1}
Noise Bandwidth ($2B_L$)		2000	cps
Time Constants	T_1	8.5	msec
	T_2	.75	msec

Input-Output Characteristics

Input Frequency	38,104	mc/sec
Input Power	+10	dbm
Output Frequency	1.171	mc/sec
Output Power (~~50~~ 18 ohm load)	+1.72 MW	~~dbm~~

DATA SHEET

AROD TRANSPONDER

Circuit Board X4.8 MULT S/N PROTOTYPE

Date 2-4-64 Test By E. Guest

RETESTED

Loop Characteristics

VCO Frequency: -ϕ VDC 5.621 243 mc/sec

0 VDC 5.620 841 mc/sec

+ϕ VDC 5.620 421 mc/sec

VCO Gain (±1VDC) 411 cps/volt

ϕ Det. "S" Curve 5.5 volts peak

ϕ Det. Gain (Calculated) .0915 volts/Deg.

ϕ Det. Balance _____ MVDC

Open Loop Gain ($360K_VK_DK_M$) 68000 sec^{-1}

Noise Bandwidth ($2B_L$) 2340 cps CALCULATED

Time Constants T_1 ≈ 14 msec

T_2 0.75 msec

Input-Output Characteristics

Input Frequency 1.171 mc/sec

Input Power _____ dbm

Output Frequency 5.620841 mc/sec

Output Power (50 ohm load) _____ dbm

TRANS SYNTH CH#1 P_{OUT} = 5.4 dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X 4.8 MULTIPLIER S/N PROTO TYPE #2

Date 4-21-64 Test By B GUEST

Loop Characteristics

VCO Frequency:	-5 VDC	5.623364	mc/sec
	0 VDC	5.620835	mc/sec
	+5 VDC	5.618250	mc/sec
VCO Gain (±1VDC)		505	cps/volt
Ø Det. "S" Curve		3.5	volts peak
Ø Det. Gain (Calculated)		.0583	volts/Deg.
Ø Det. Balance		± 20	MVDC
Open Loop Gain ($360K_VK_DK_M$)		52500	sec^{-1}
Noise Bandwidth ($2B_L$)		2000	cps
Time Constants	T_1	14.22	msec
	T_2	.75	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	0	dbm
Output Frequency	5.6208	mc/sec
Output Power (50 ohm load)	+10	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board V 6 MULT S/N PROTO TYPE

Date 1-6-64 Test By C BOARD

Loop Characteristics

VCO Frequency:	-5 VDC	7.022847	mc/sec
	0 VDC	7.025991	mc/sec
	+5 VDC	7.029245	mc/sec
VCO Gain (±1VDC)		530	cps/volt
Ø Det. "S" Curve		5	volts peak
Ø Det. Gain (Calculated)		.0666	volts/Deg.
Ø Det. Balance		50 MAX	MVDC
Open Loop Gain ($360K_VK_DK_M$)		[illegible]	sec^{-1}
Noise Bandwidth ($2B_L$)		2,100	cps CALCULATED
Time Constants	T_1	21.05	msec
	T_2	.75	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	6	dbm
Output Frequency	7,026	mc/sec
Output Power (50 ohm load)	+6	dbm

Test [illegible] sys Tx CH 2 P_{out} = [illegible]

DATA SHEET

AROD TRANSPONDER

Circuit Board X6 Mult. 362150 S/N 2

Date 4-22-64 Test By Byd

Loop Characteristics

VCO Frequency:	-$ VDC	7.026361	mc/sec
	0 VDC	7.026004	mc/sec
	+$ VDC	7.025150	mc/sec
VCO Gain (±1VDC)		800	cps/volt
Ø Det. "S" Curve			volts peak
Ø Det. Gain (Calculated)			volts/Deg.
Ø Det. Balance			DC
Open Loop Gain ($360K_VK_DK_M$)		5,000	
Noise Bandwidth ($2B_L$)		2000	cps
Time Constants	T	15.75	msec
	T^2	0.75	msec

Input-Output Characteristics

Input Frequency	1.171 mc	mc/sec
Input Power	0 dbm	dbm
Output Frequency	7.0625 mc	c/sec
Output Power (50 ohm load)	+10	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X10.6 MULTIPLIER S/N PROTOTYPE

Date [illegible] Test By B Hunt

Loop Characteristics

VCO Frequency:	-5 VDC	12.418134	mc/sec
	0 VDC	12.412042	mc/sec
	+5 VDC	12.405938	mc/sec
VCO Gain (±1VDC)		1419	cps/volt
Ø Det. "S" Curve		2.5	volts peak
Ø Det. Gain (Calculated)		.0417	volts/Deg.
Ø Det. Balance		± 20 (max)	MVDC
Open Loop Gain ($360K_VK_DK_M$)		106,500	sec^{-1}
Noise Bandwidth ($2B_L$)		2400	cps CALCULATED
Time Constants	T_1	21	msec
	T_2	.57	msec

Input-Output Characteristics

Input Frequency	1.131	mc/sec
Input Power	0	dbm
Output Frequency	12.412	mc/sec
Output Power (50 ohm load)	[illegible]	dbm

TX [illegible] #2, CHAN #3 P_{OUT} = +4.0 DBM

DATA SHEET

AROD TRANSPONDER

Circuit Board _____ S/N _____

Date _____ Test By _____

Loop Characteristics

VCO Frequency: -5 VDC _____ mc/sec

0 VDC _____ mc/sec

+5 VDC _____ mc/sec

VCO Gain (±1VDC) _____ cps/volt

ϕ Det. "S" Curve _____ volts peak

ϕ Det. Gain (Calculated) _____ volts/Deg.

ϕ Det. Balance _____ MVDC

Open Loop Gain ($360K_VK_DK_M$) _____ sec^{-1}

Noise Bandwidth ($2B_L$) _____ cps

Time Constants τ_1 _____ msec

τ_2 _____ msec

Input-Output Characteristics

Input Frequency _____ mc/sec

Input Power _____ dbm

Output Frequency _____ mc/sec

Output Power (50 ohm load) _____ dbm

DATA SHEET

AROD TRANSPONDER #1

Circuit Board X 11.8 Mult S/N Prototype with bottom plate

Date 1-23-64 Test By C.T. Byrd Jr

Loop Characteristics

VCO Frequency:	-5 VDC	13.824170	mc/sec
	0 VDC	13.817805	mc/sec
	+5 VDC	13.807635	mc/sec
VCO Gain (±1VDC)		1.00	cps/volt (±3VDC)
Ø Det. "S" Curve		2.5	volts peak
Ø Det. Gain (Calculated)		0.0417	volts/Deg.
Ø Det. Balance		-20	MVDC
Open Loop Gain ($360K_VK_DK_M$)		121.500	sec^{-1}
Noise Bandwidth ($2B_L$)		3240	cps CALCULATED
Time Constants	T_1	13.	msec
	T_2	0.51	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	0	dbm
Output Frequency	13.8178	mc/sec
Output Power (50 ohm load)	+9.6	dbm
Input current (+20°)	48	ma.

TRANS. SYNTH #2 CHAN #4 P_{OUT} = +4.0 DBM

DATA SHEET

AROD TRANSPONDER

Circuit Board [illegible] S/N [illegible]

Date [illegible] Test By [illegible]

Loop Characteristics

VCO Frequency:	-5 VDC	[illegible] mc/sec
	0 VDC	[illegible] mc/sec
	+5 VDC	[illegible] mc/sec
VCO Gain (±1VDC)		[illegible] cps/volt
ϕ Det. "S" Curve		[illegible] volts peak
ϕ Det. Gain (Calculated)		[illegible] volts/Deg.
ϕ Det. Balance		[illegible] MVDC
Open Loop Gain (360K+j3KB@1K)		[illegible] sec^{-1}
Noise Bandwidth (3dB)		[illegible] cps
Time Constants	τ_1	[illegible] msec
	τ_2	[illegible] msec

Input-Output Characteristics

Input Frequency		[illegible] mc/sec
Input Power		[illegible] dbm
Output Frequency		[illegible] mc/sec
Output Power (50 ohm load)		[illegible] dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X57 MULTIPLIER S/N PROTOTYPE

Date JAN 28, 1964 Test By B Grant

Loop Characteristics

VCO Frequency: -5 VDC	22.257791	mc/sec
0 VDC	22.247456	mc/sec
+5 VDC	22.236502	mc/sec
VCO Gain (±1VDC)	2129	cps/volt
Ø Det. "S" Curve	±5	volts peak
Ø Det. Gain (Calculated)	.0573	volts/Deg.
Ø Det. Balance	+50 MAX	MVDC
Open Loop Gain ($360K_VK_DK_M$)	63520	sec^{-1}
Noise Bandwidth ($2B_L$)	1682	cps
Time Constants τ_1	27	msec
τ_2	1	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	+10	dbm
Output Frequency	66.747	mc/sec
Output Power (50 ohm load)	+10.8	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X57 S/N Prototype #2

Date [illegible] Test By [illegible]

Loop Characteristics

VCO Frequency:	-5 VDC	[illegible]	mc/sec
	0 VDC	[illegible]	mc/sec
	+5 VDC	[illegible]	mc/sec
VCO Gain (±1VDC)		[illegible]	cps/volt
∅ Det. "S" Curve		[illegible]	volts/rad
∅ Det. Gain (Calculated)		[illegible]	volts/rad
∅ Det. Balance		[illegible]	mV
Open Loop Gain ($\omega_{OL}=K_VK_DK_M$)		[illegible]	sec^{-1}
Noise Bandwidth ($2B_L$)		[illegible]	cps
Time Constants	τ_1	[illegible]	msec
	τ_2	[illegible]	msec

Input-Output Characteristics

Input Frequency	1.1721	mc/sec
Input Power	-7[illegible]	dbm
Output Frequency	61.2412	mc/sec
Output Power (50 ohm load)	[illegible]	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X58 Multiplier S/N Prototype 1

Date Feb. 4, 1964 Test By C.T. Byrd J.

Loop Characteristics

VCO Frequency:	-5 VDC	33.962 007	mc/sec
	0 VDC	33.959060	mc/sec
	+5 VDC	33.956 125	mc/sec
VCO Gain (±1VDC)		6.0	cps/volt
Ø Det. "S" Curve		.25	volts peak
Ø Det. Gain (Calculated)		.125	volts/Deg.
Ø Det. Balance		60	MVDC
Open Loop Gain ($360K_VK_DK_M$)		28,000	sec^{-1}
Noise Bandwidth ($2B_L$)		1244	cps
Time Constants	τ_1	20.4	msec
	τ_2	1.8	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	0	dbm
Output Frequency	62.918000	mc/sec
Output Power (50 ohm load)	+13	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X 56 S/N Beta Type No 2

Date [illegible] Test By [illegible]

Loop Characteristics

VCO Frequency:	-5 VDC	[illegible]	mc/sec
	0 VDC	[illegible]	mc/sec
	+5 VDC	[illegible]	mc/sec
VCO Gain (±1VDC)		[illegible]	cps/volt
∅ Det. "S" Curve		[illegible]	volts peak
∅ Det. Gain (Calculated)		[illegible]	volts/rad.
∅ Det. Balance		[illegible]	MVDC
Open Loop Gain ($360K_VK_DK_M$)		[illegible]	sec^{-1}
Noise Bandwidth ($2B_L$)		[illegible]	cps
Time Constants	T_1	[illegible]	msec
	T_2	[illegible]	msec

Input-Output Characteristics

Input Frequency	[illegible]	mc/sec
Input Power	-20	dbm
Output Frequency	47.9[illegible]	mc/sec
Output Power (50 ohm load)	[illegible]	dbm

[illegible]

DATA SHEET

AROD TRANSPONDER

Circuit Board Y60 MULTIPLIER S/N PROTO TYPE

Date FEB 15, 1964 Test By P Ghost

Loop Characteristics

VCO Frequency:	-5 VDC	70,263754	mc/sec
	0 VDC	70,260326	mc/sec
	+5 VDC	70,255840	mc/sec
VCO Gain (±1VDC)		750	cps/volt
Ø Det. "S" Curve		3	volts peak
Ø Det. Gain (Calculated)		.65	volts/Deg.
Ø Det. Balance			MVDC
Open Loop Gain ($360K_VK_DK_M$)		131000	sec^{-1}
Noise Bandwidth ($2B_L$)		5200	cps
Time Constants	T_1	5.46	msec
	T_2	.36	msec

Input-Output Characteristics

Input Frequency	1.171 ~~HF~~ mc	mc/sec
Input Power	Ecliomorgreaker	dbm
Output Frequency	70.26	mc/sec
Output Power (50 ohm load)	+ 8.8	dbm

DC AMP GAIN — 4.67

DATA SHEET

AROD TRANSPONDER

Circuit Board X60 MULT S/N PROTOTYPE #2

Date 11-10-64 Test By [illegible]

Loop Characteristics

VCO Frequency:	-5 VDC	[illegible]	mc/sec
	0 VDC	[illegible]	mc/sec
	+5 VDC	[illegible]	mc/sec
VCO Gain (±1VDC)		87	cps/volt
∅ Det. "S" Curve		3	volts peak
∅ Det. Gain (Calculated)		.477	volts/Deg.
∅ Det. Balance		[illegible]	MVDC
Open Loop Gain ($360K_VK_DK_M$)		[illegible]	sec^{-1}
Noise Bandwidth ($2B_L$)		[illegible]	cps
Time Constants	τ_1	[illegible]	msec
	τ_2	.340	msec

Input-Output Characteristics

Input Frequency	1171	mc/sec
Input Power	0	dbm
Output Frequency	70.36	mc/sec
Output Power (50 ohm load)	+10.6	dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board X 76 S/N PROTOTYPE

Date 2-27-64 Test By B Guest

Loop Characteristics

VCO Frequency:	-5 VDC	89.001866	mc/sec
	0 VDC	88.996397	mc/sec
	+5 VDC	88.988493	mc/sec
VCO Gain (±1VDC)		1322	cps/volt
Ø Det. "S" Curve		3.2	volts peak
Ø Det. Gain (Calculated)		.0533	volts/Deg.
Ø Det. Balance		50 MAX	MVDC
DC AMP GAIN		4.5	
Open Loop Gain ($360K_VK_DK_M$)		228500	sec^{-1}
Noise Bandwidth ($2B_L$)		1604	cps
Time Constants	T_1	~~44~~ 100	msec
	T_2	1	msec

Input-Output Characteristics

Input Frequency	1.171	mc/sec
Input Power	0	dbm
Output Frequency	88.996	mc/sec
Output Power (50 ohm load)		dbm

DATA SHEET

AROD TRANSPONDER

Circuit Board Y 26 S/N PROTOTYPE # 2

Date 4-20-64 Test By R. GUEST

Loop Characteristics

VCO Frequency:	-5 VDC	89.003330	mc/sec
	0 VDC	[illegible]	mc/sec
	+5 VDC	[illegible]	mc/sec
VCO Gain (±1VDC)		[illegible]	cps/volt
Ø Det. "S" Curve		[illegible]	volts peak
Ø Det. Gain (Calculated)		.0563	volts/Deg.
Ø Det. Balance		[illegible]	MVDC
Open Loop Gain ($360K_VK_DK_M$)		[illegible]	sec^{-1}
Noise Bandwidth ($2B_L$)		4000	cps
Time Constants	T_1	33.3	msec
	T_2	.375	msec

Input-Output Characteristics

Input Frequency	1.121	mc/sec
Input Power	0	dbm
Output Frequency	88.996	mc/sec
Output Power (50 ohm load)	+10	dbm